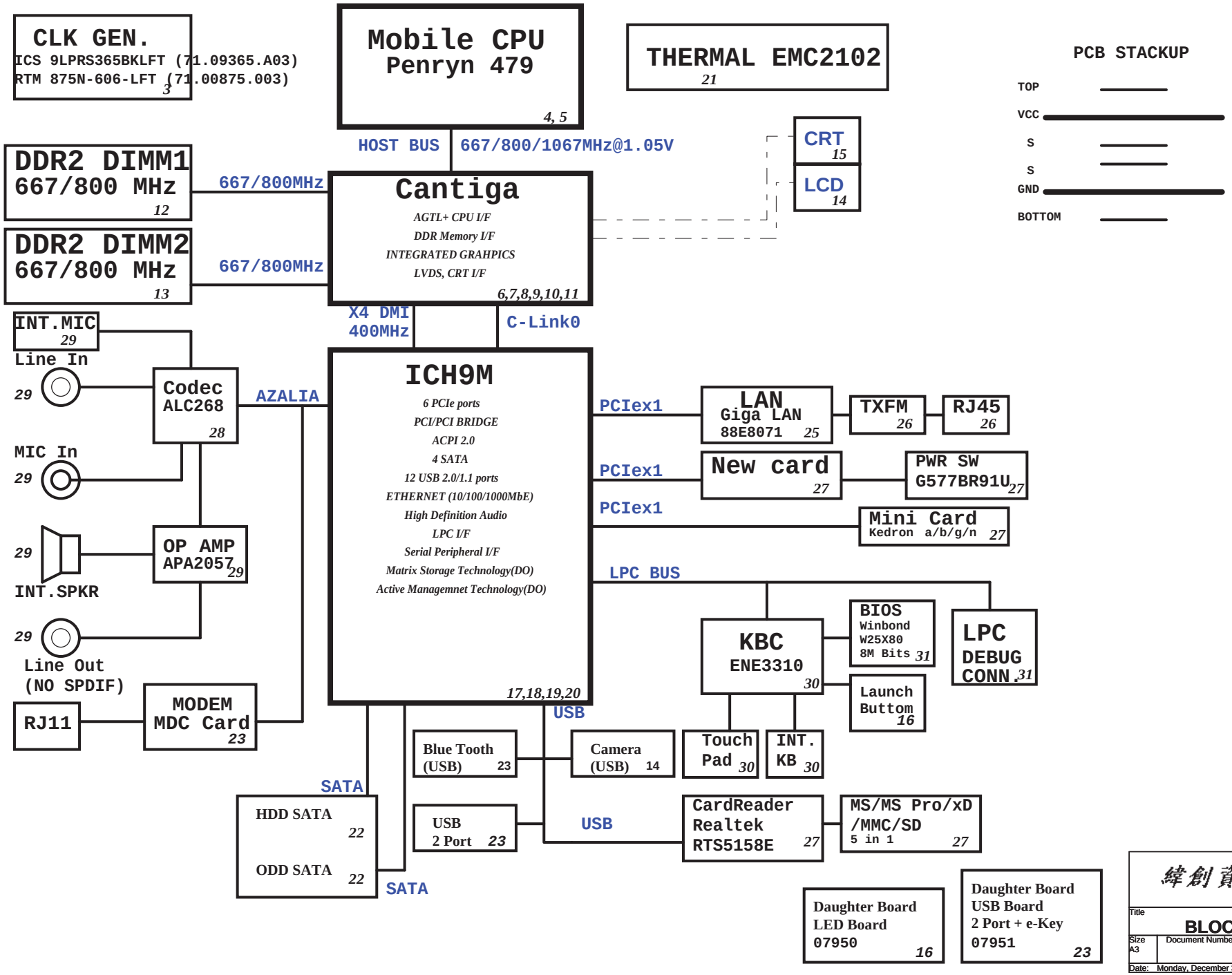
Cathedral Peak Block Diagram

Project code: 91.4J501.001
PCB P/N : 48.4J501.001
REVISION : 07261



PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 44	
1D8V_S3	1D5V_S0

CFXCORE DC/DC ISL6263 35,36	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24750 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title		
BLOCK DIAGRAM		
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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

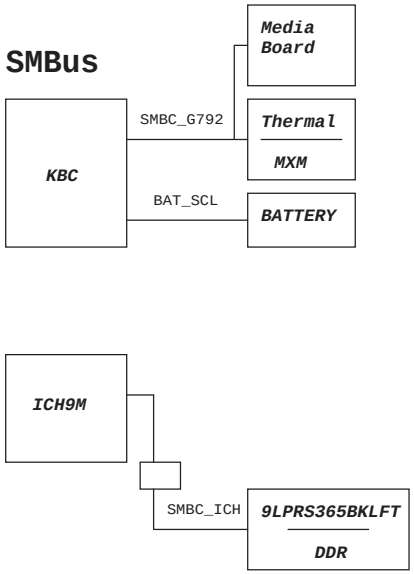
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	NC
4	USB3
5	Bluetooth
6	NC
7	MINIC1
8	WEBCAM
9	NEW1
10	Card Reader
11	NC

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Title: Reference

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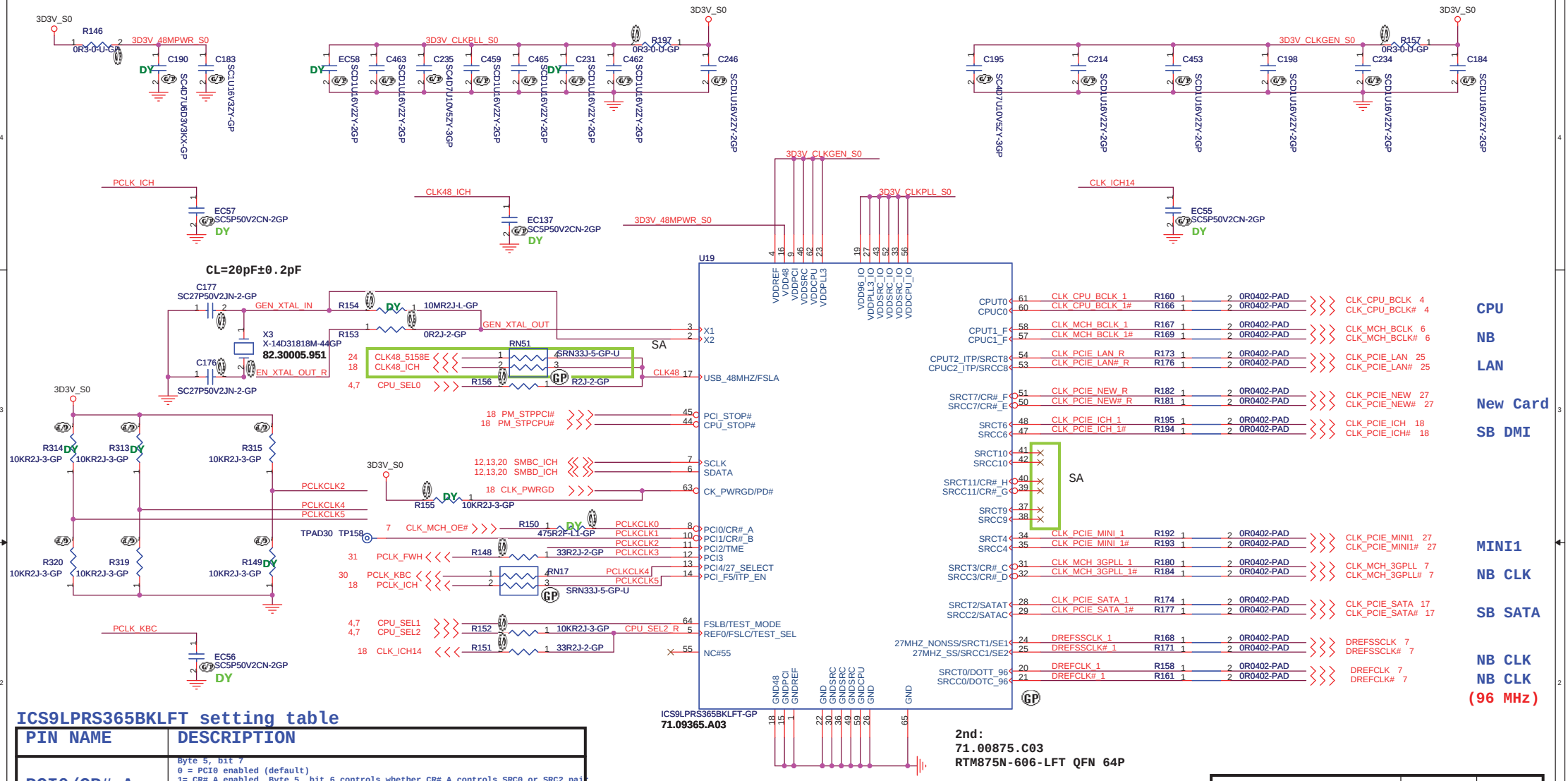

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

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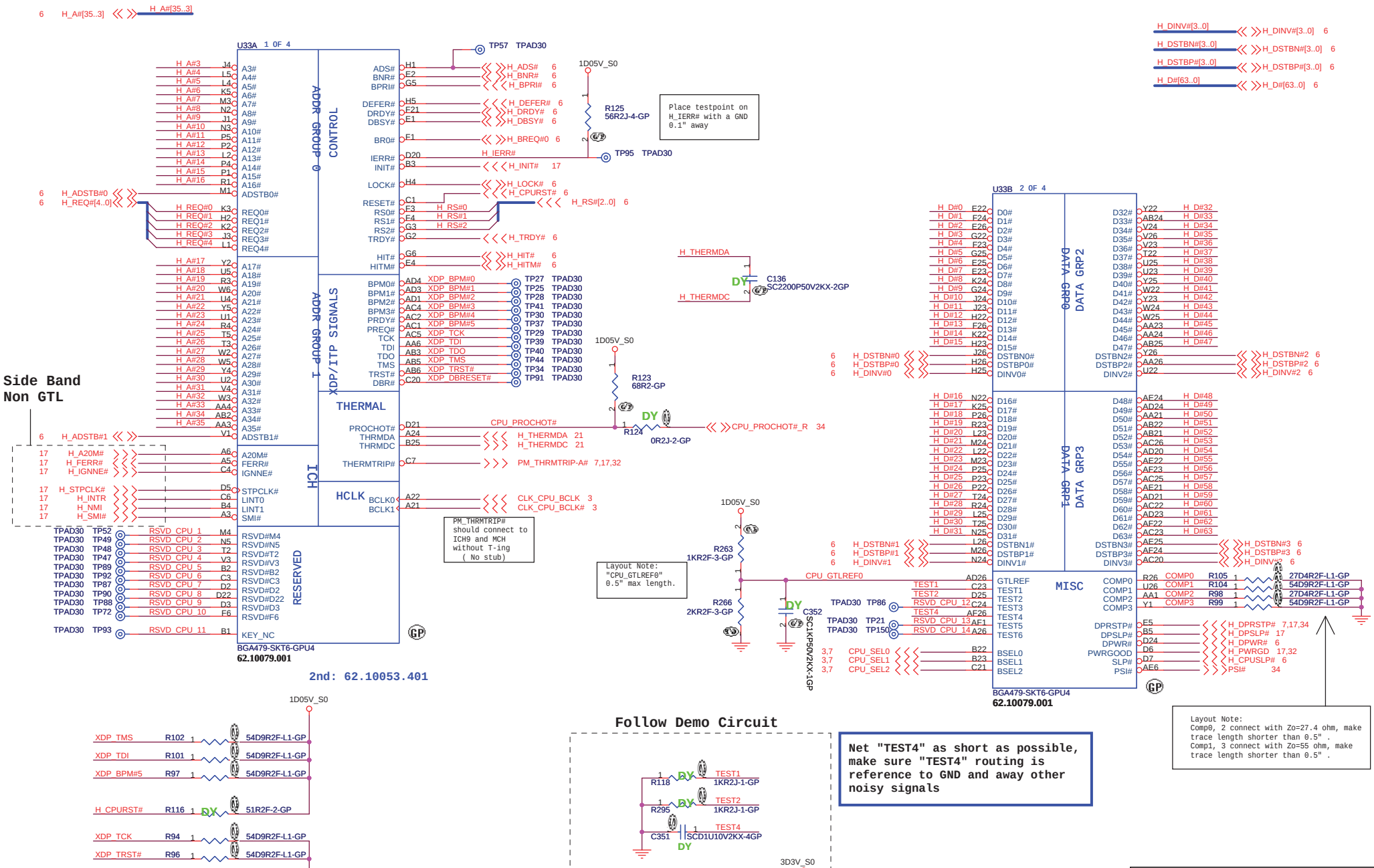

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Title: CPU (1 of 2)

Size | Document Number: Cathedral Peak | Rev: SA

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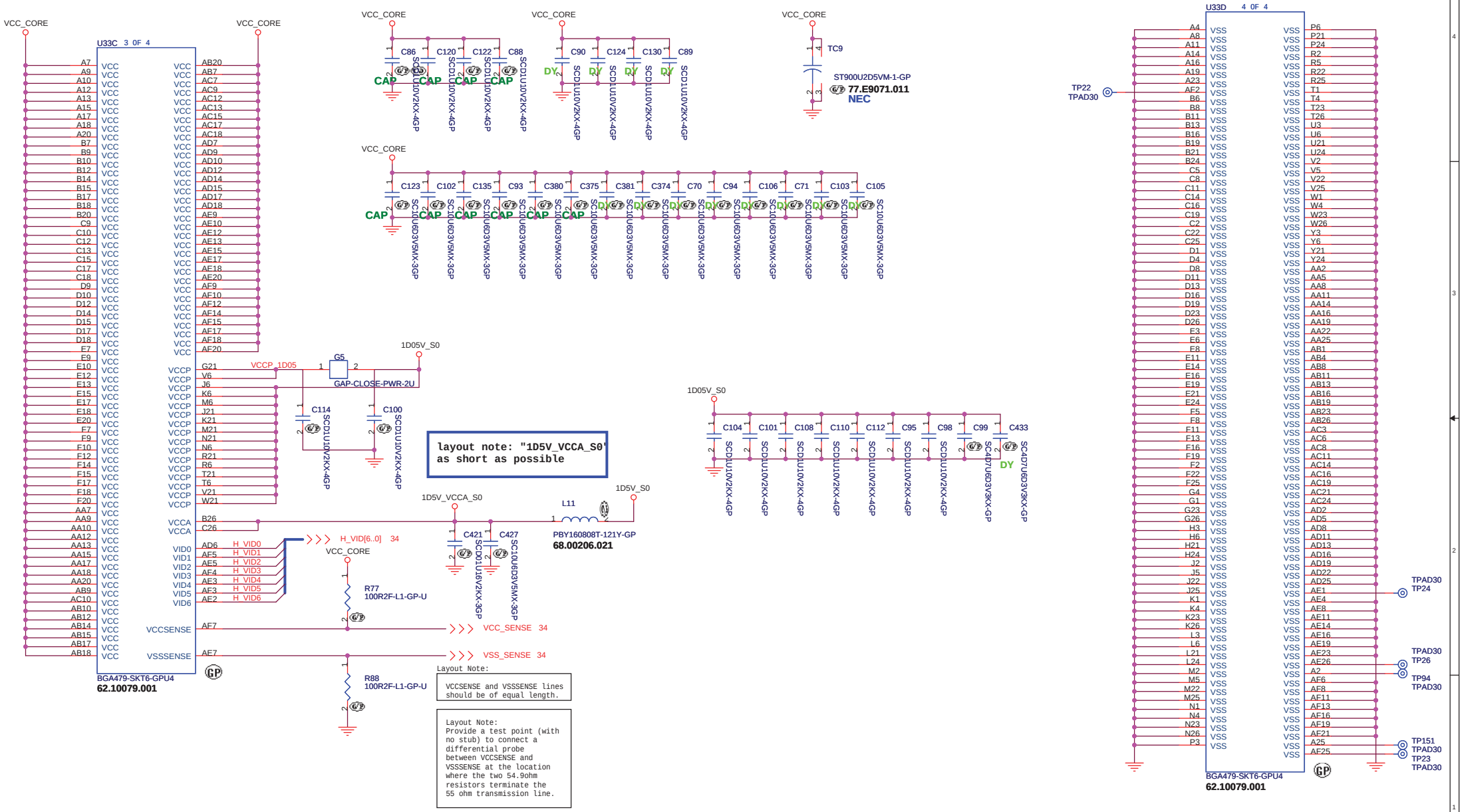

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Title		
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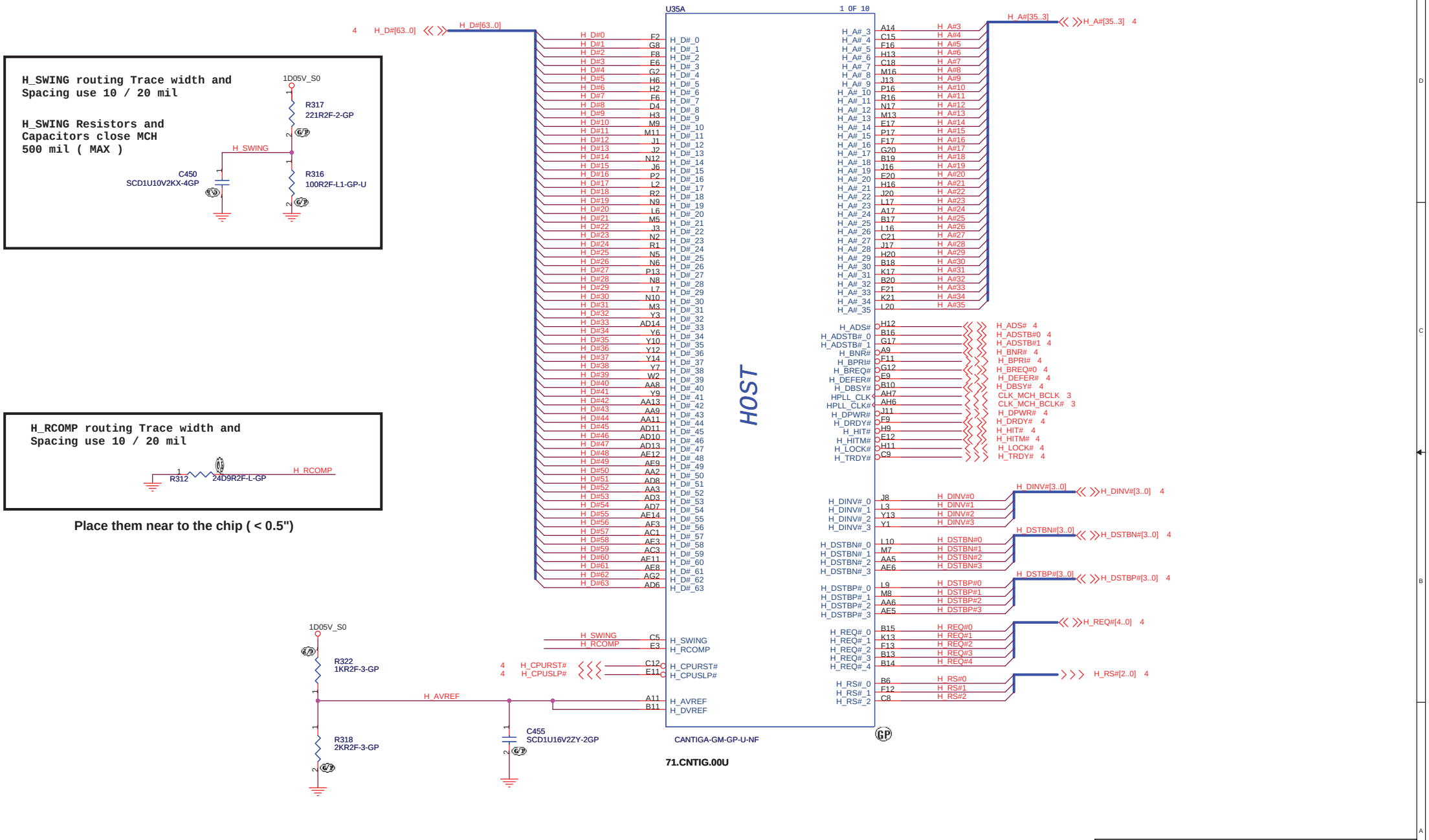

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Title: Cantiga (1 of 6)

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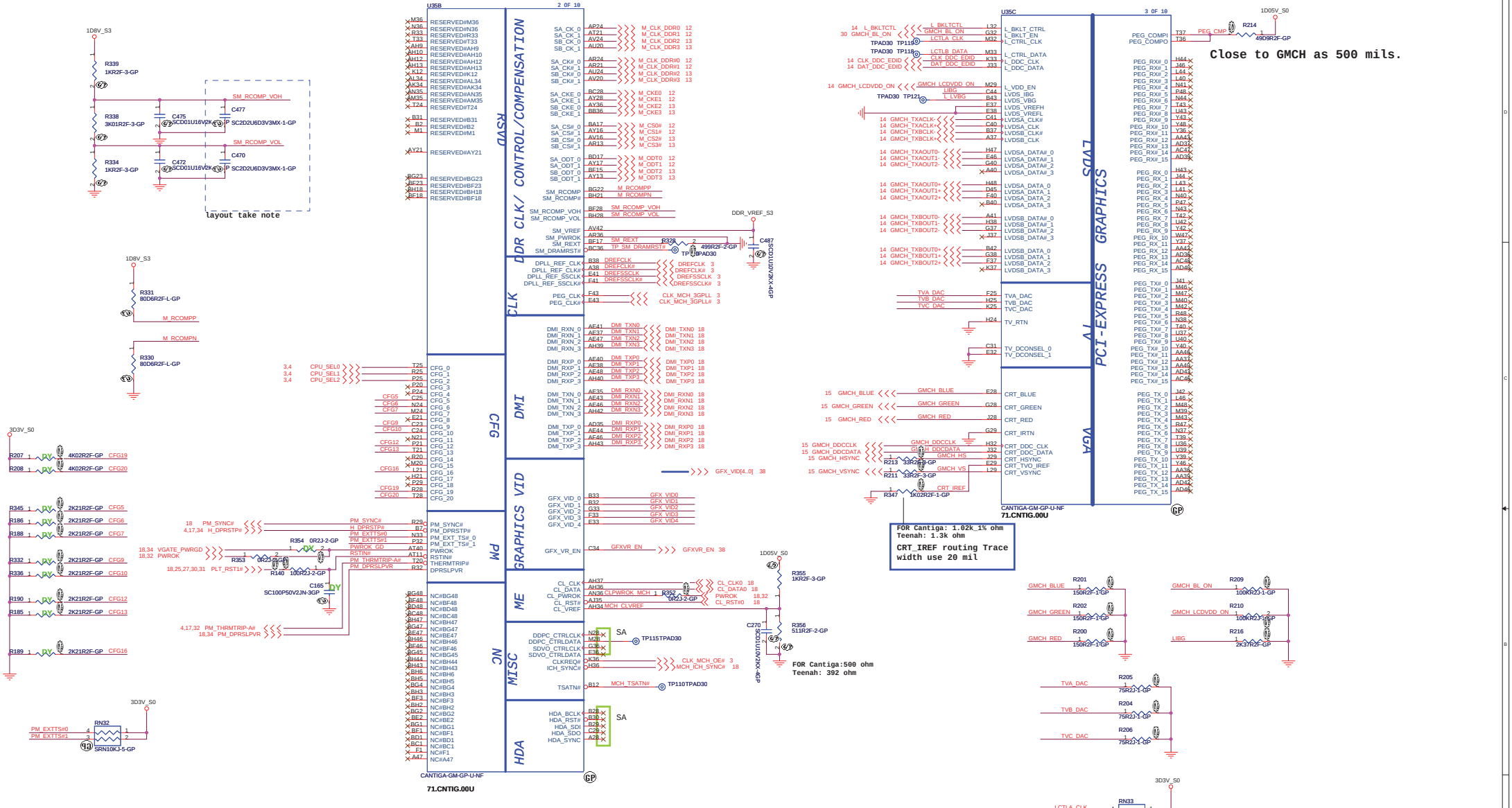

Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

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Title: Cantiga (2 of 6)

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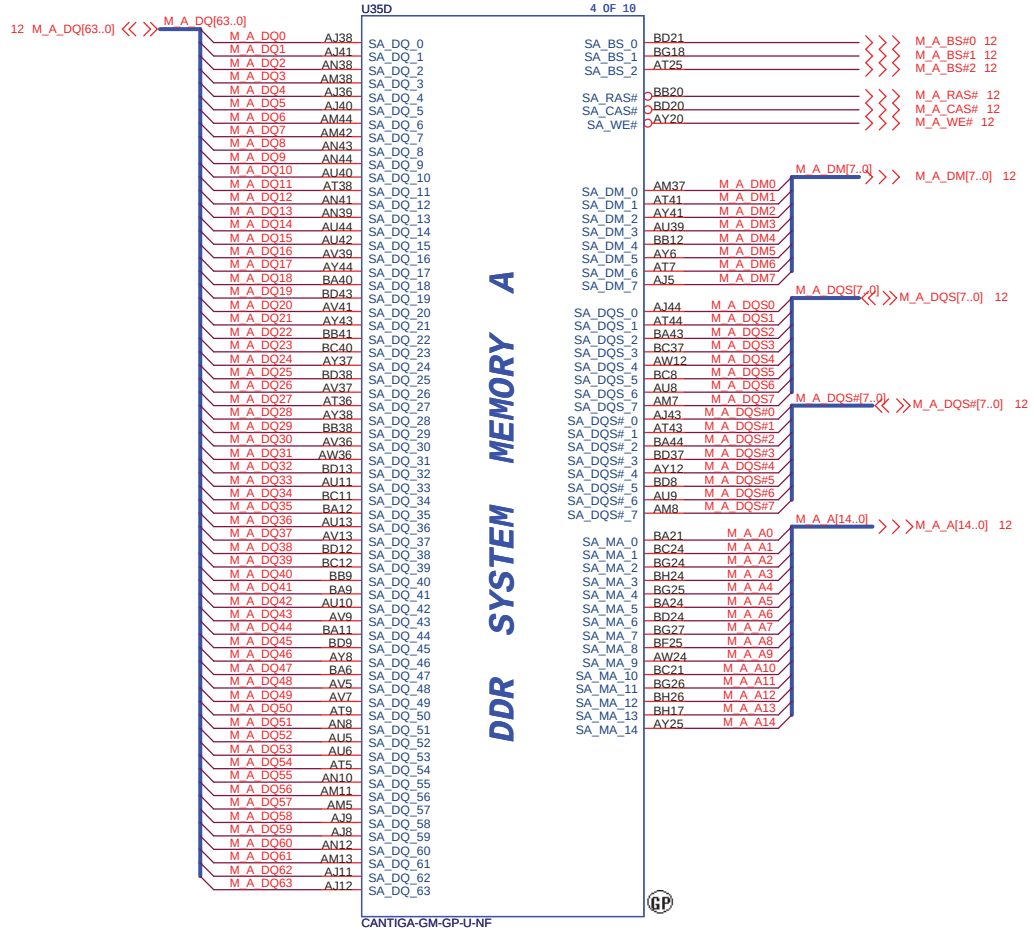

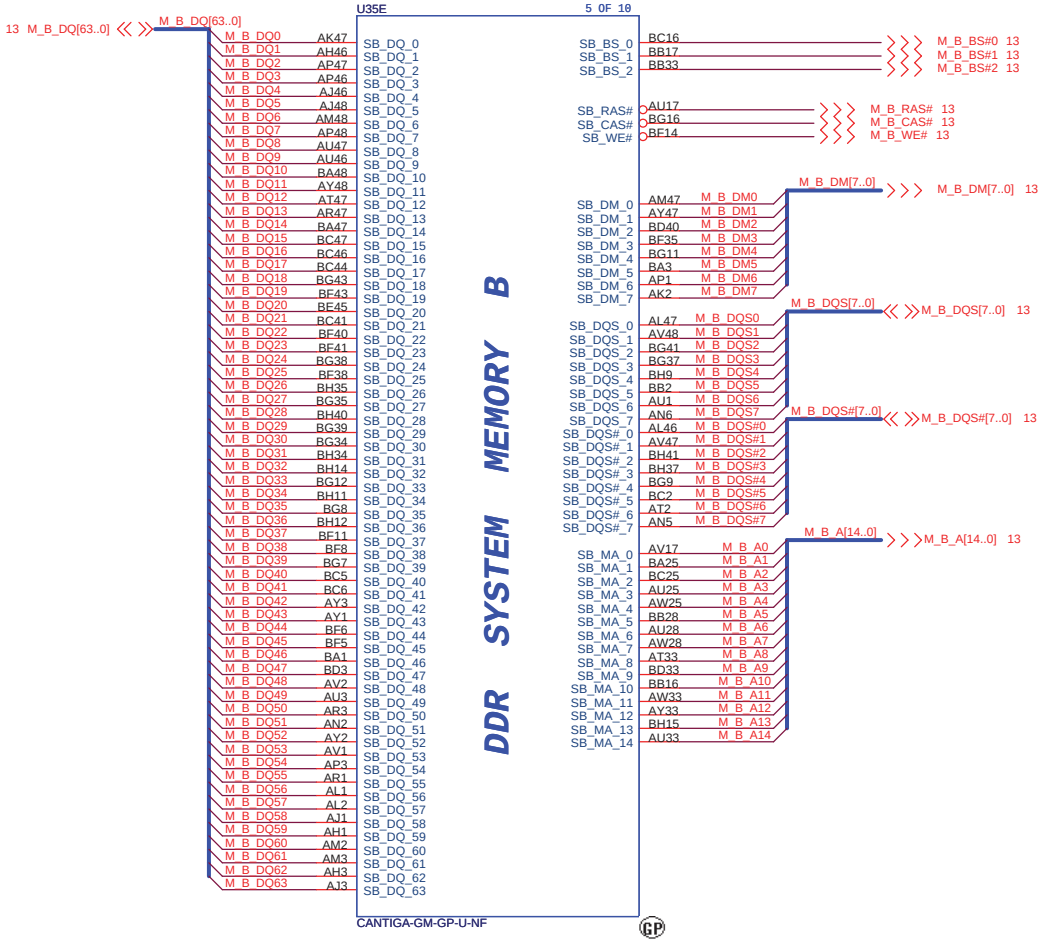

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Title	**Cantiga (3 of 6)**	
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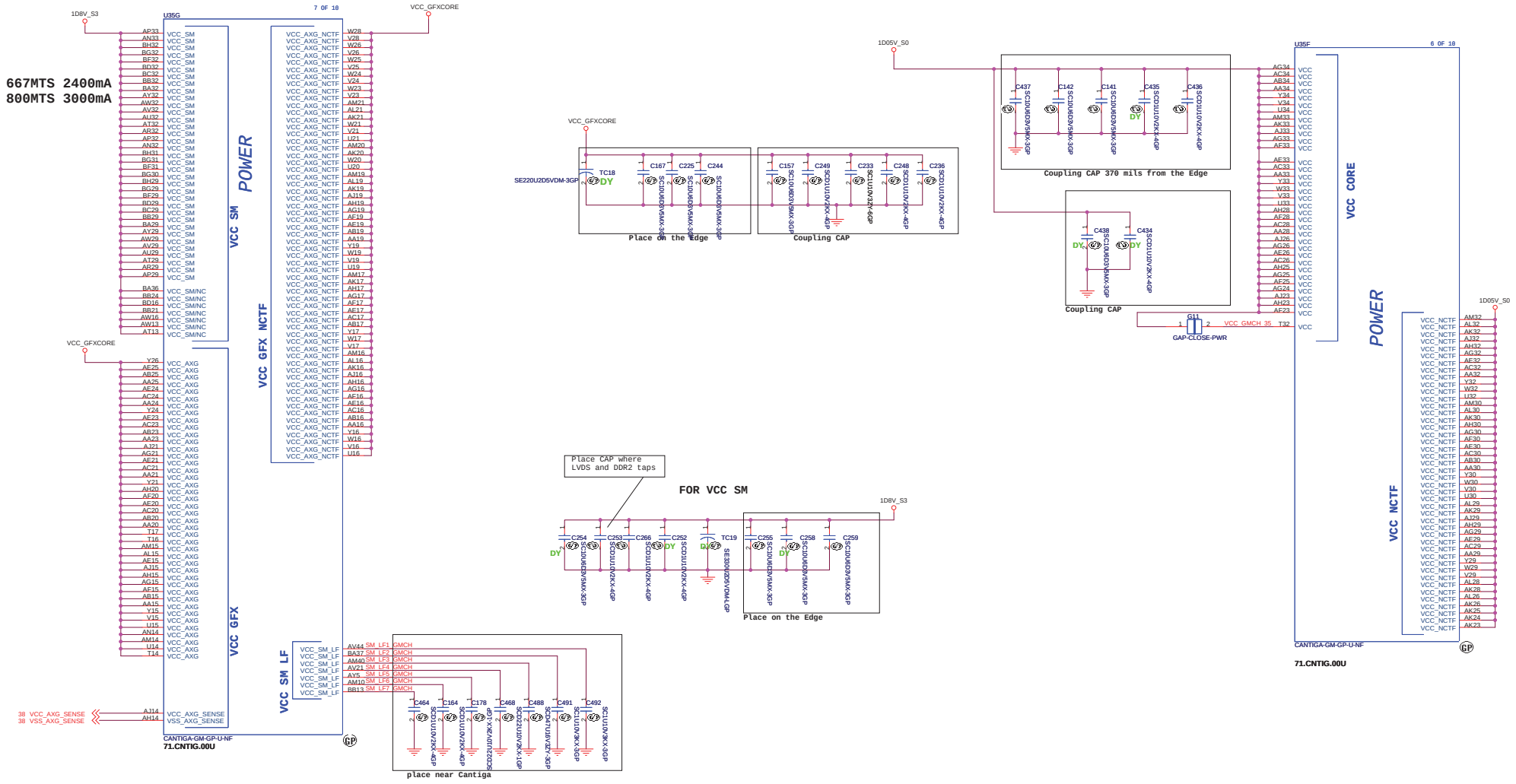

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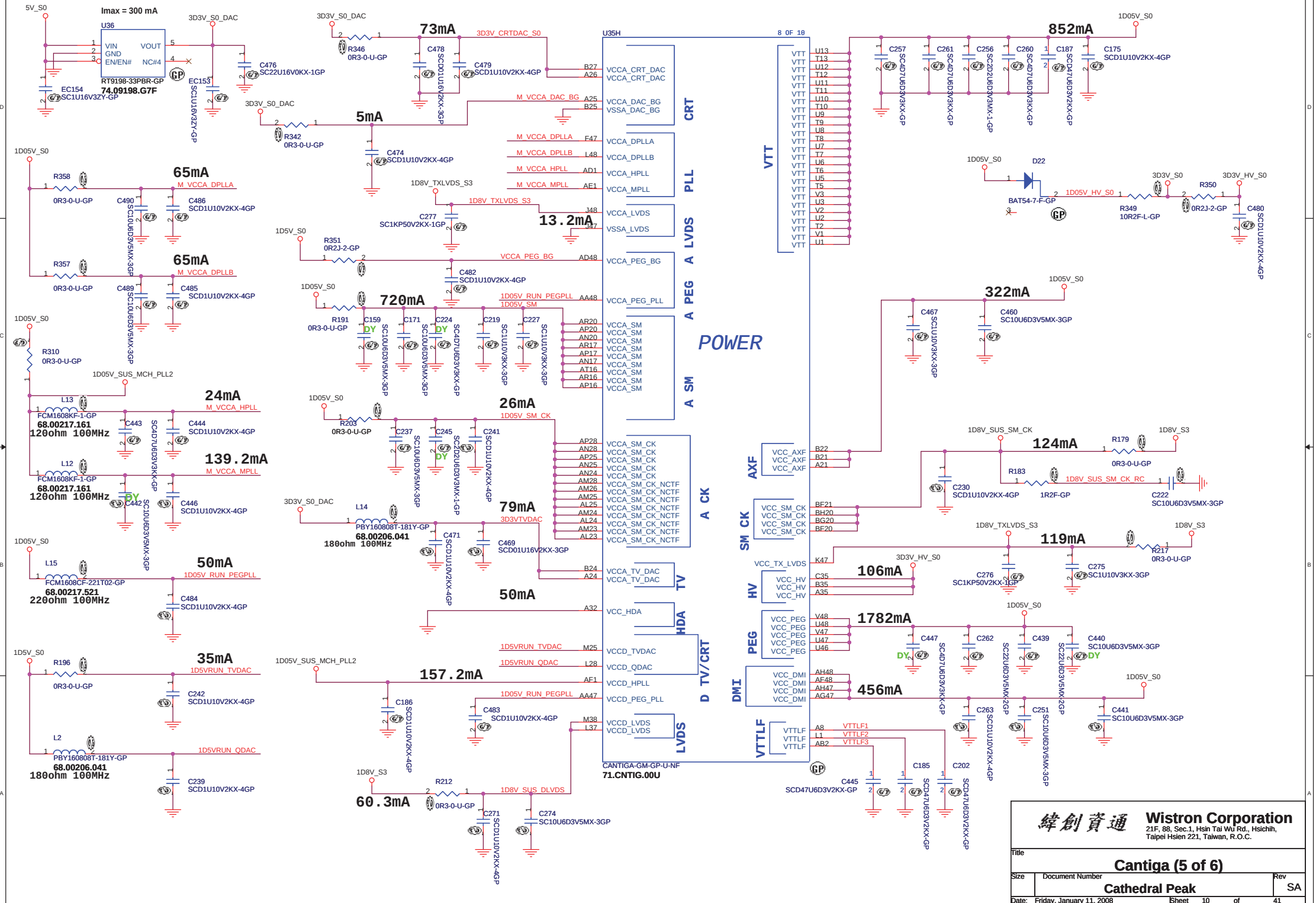
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EC153
SC1U16V3ZY-GP
C476
SC22U16V0KX-1GP
73mA
R346
0R3-0-U-GP
C478
SCD1U16V2KX-3GP
C479
SCD1U10V2KX-4GP
3D3V_CRTDAC_S0
5mA
R342
0R3-0-U-GP
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R212
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C274
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U35H
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VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_CK
VCCA_SM_CK_NCTF
VCCA_TV_DAC
VCCA_TV_DAC
VCC_HDA
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
VCCD_LVDS
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
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SM CK
HV
PEG
DMI
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VCC_SM_CK
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VCC_HV
VCC_PEG
VCC_DMI
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VTTLF2
VTTLF3
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C261
SC4D7U6D3V3KX-GP
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D22
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R349
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3D3V_HV_S0
R350
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C202
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緯創資通
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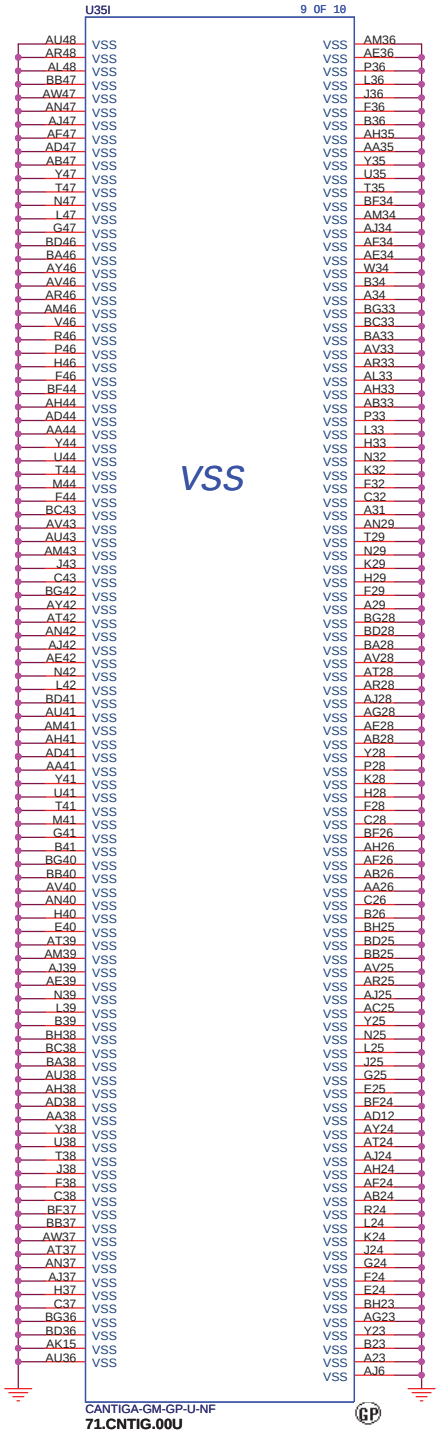
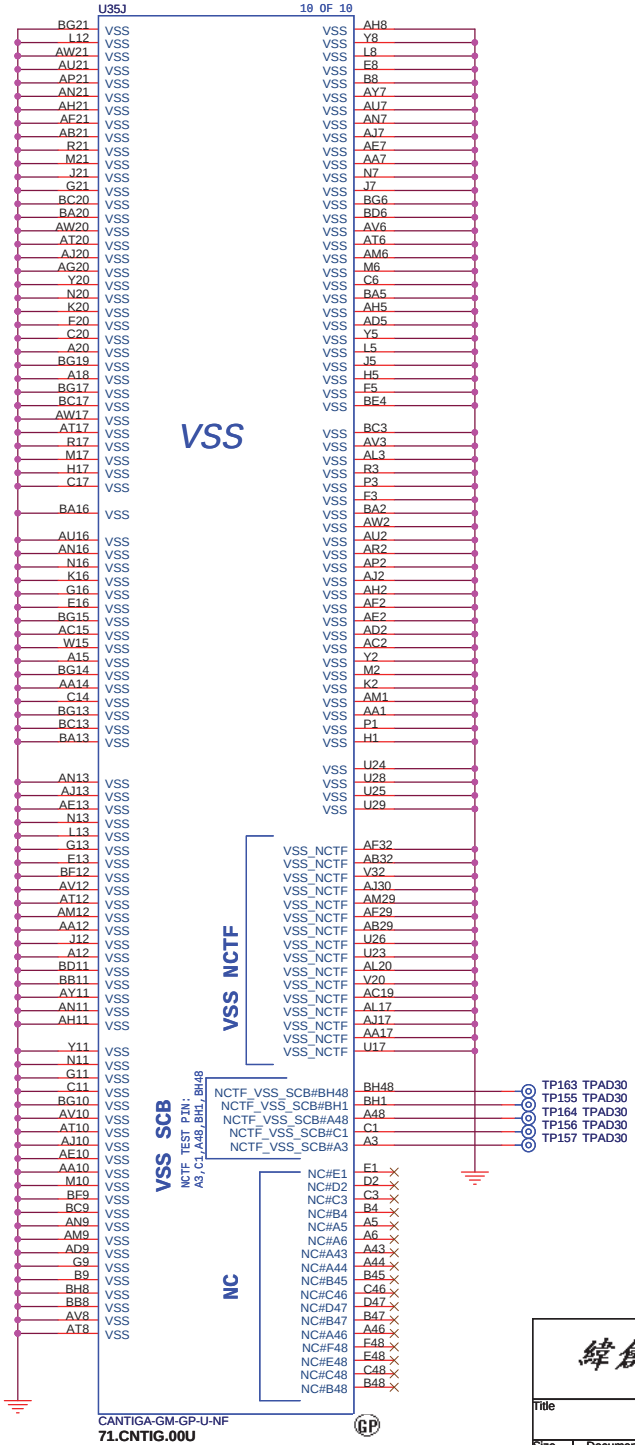
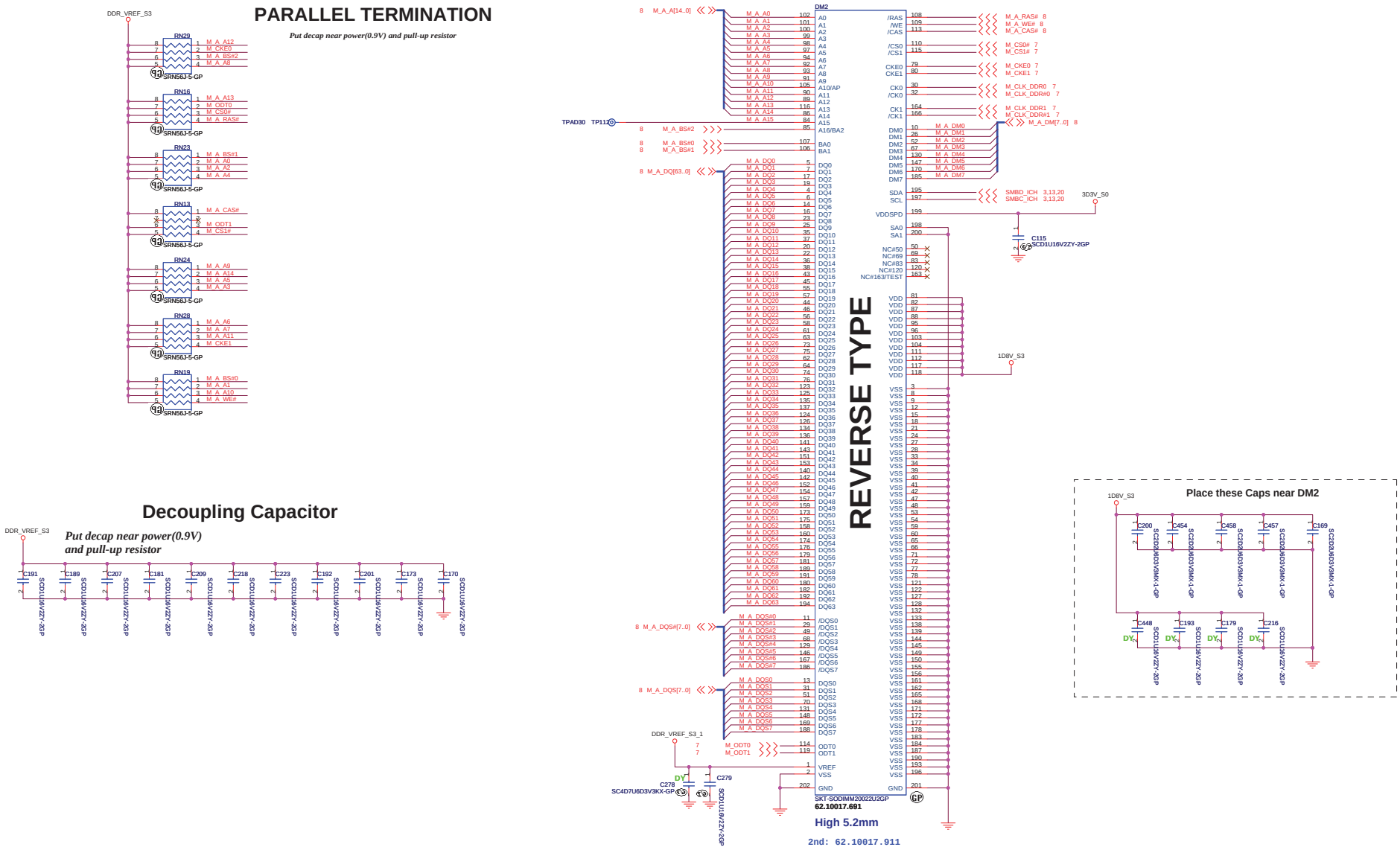


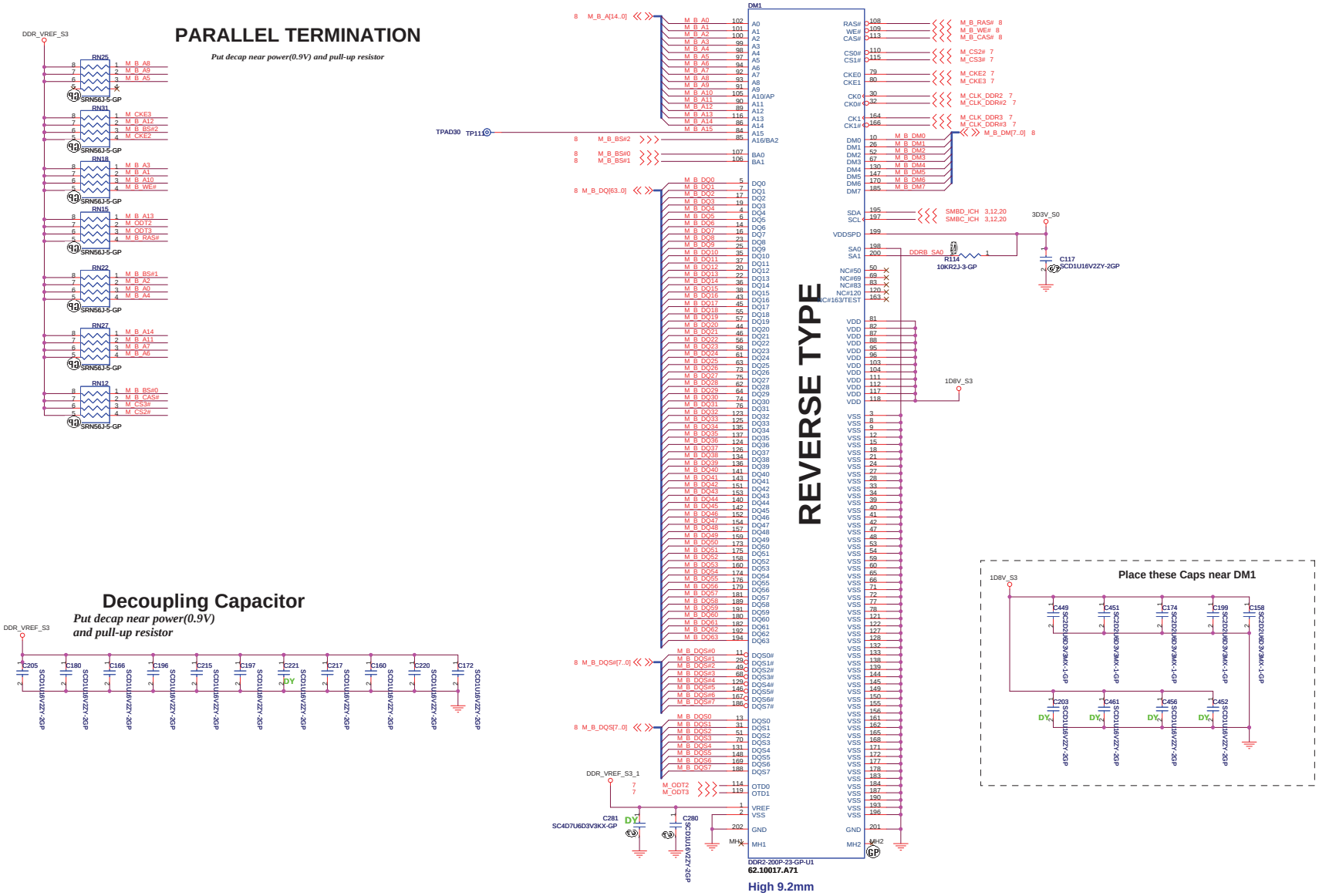


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Cantiga (6 of 6)**	
Size	Document Number: **Cathedral Peak**	Rev: SA
Date: Friday, January 11, 2008	Sheet 11 of 41	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DDR2 Socket 1 (DM2)**
Size / Document Number	**Cathedral Peak**
Rev	SA
Date: Friday, January 11, 2008	Sheet 12 of 41



緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 Socket 0 (DM1)**

Size	Document Number	Rev
	Cathedral Peak	SA

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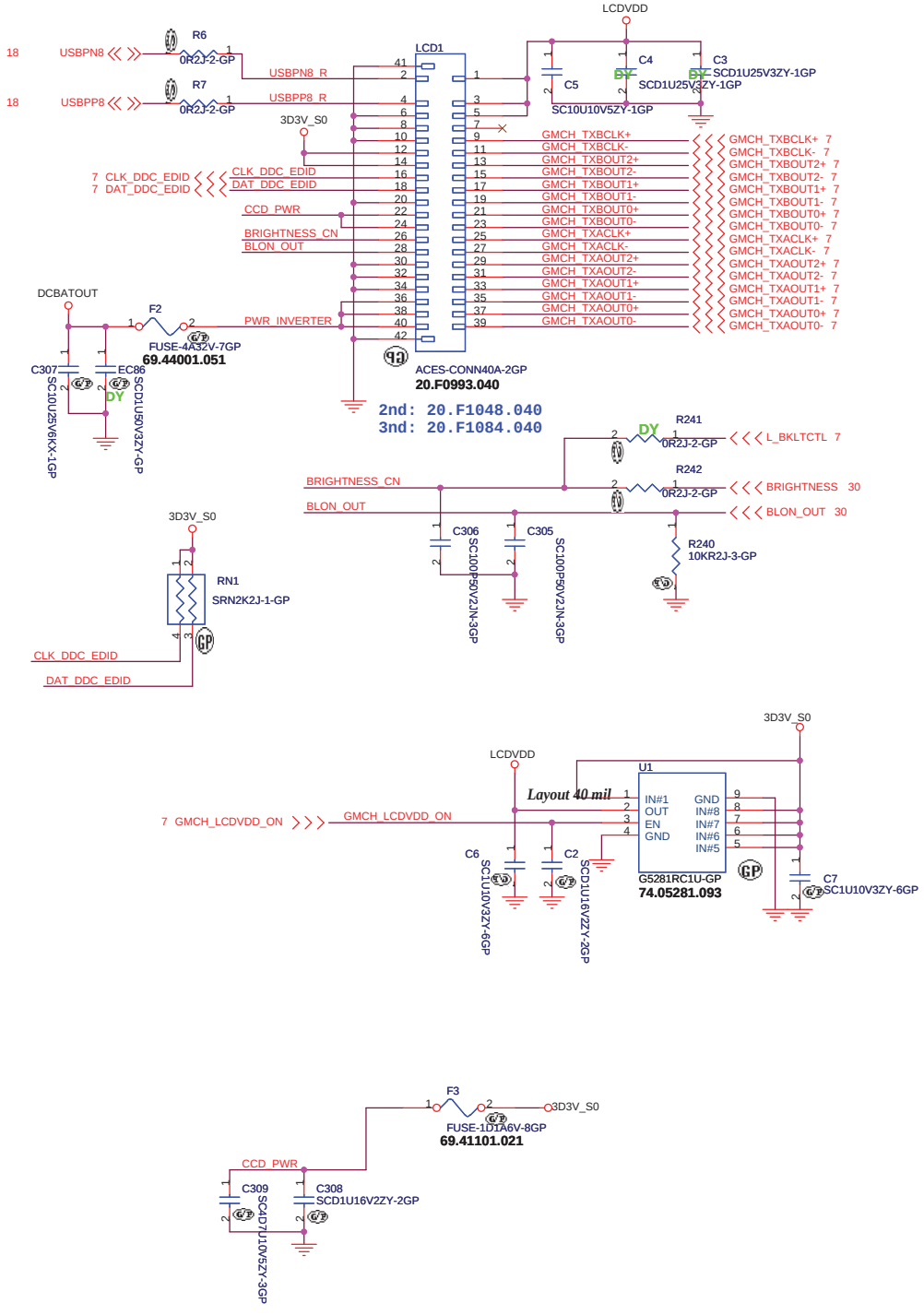
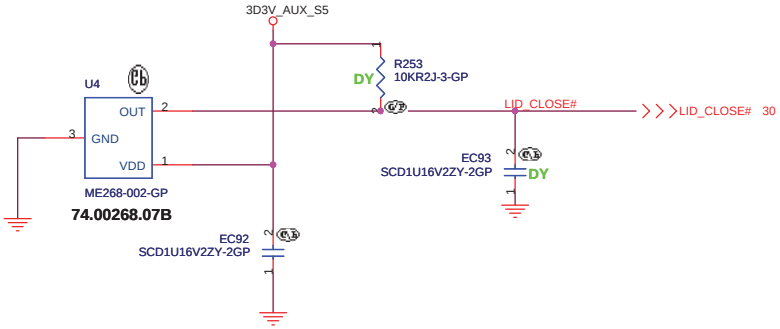
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

Cover Up Switch



74.00268.A7B
74.00268.C7B

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size | Document Number: Cathedral Peak | Rev: SA

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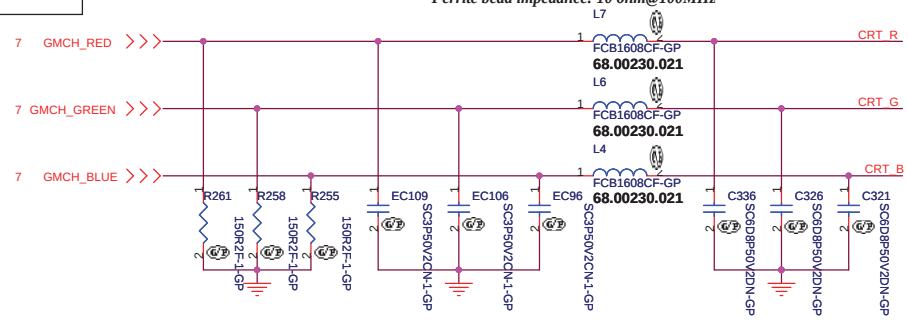
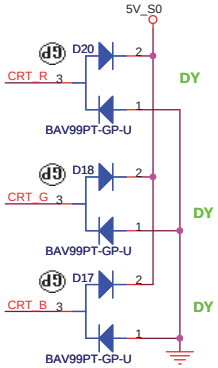
Layout Note:
Place these resistors
close to the CRT-out
connector

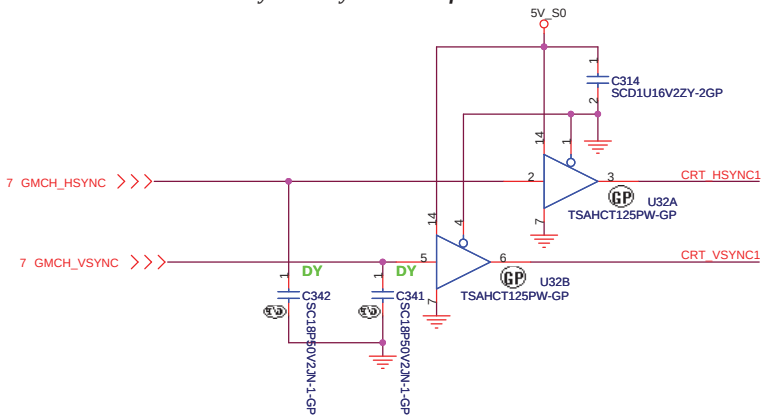
Ferrite bead impedance: 10 ohm@100MHz



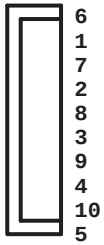


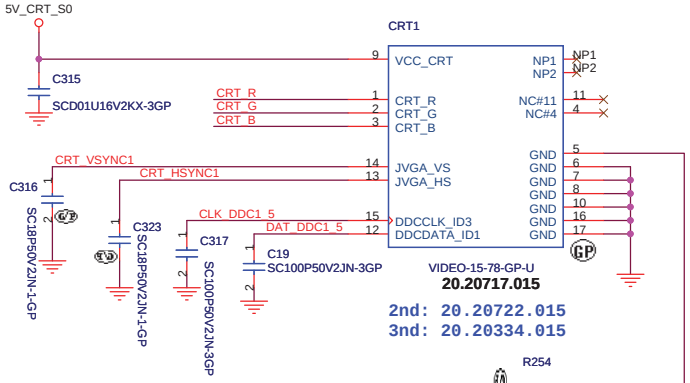
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

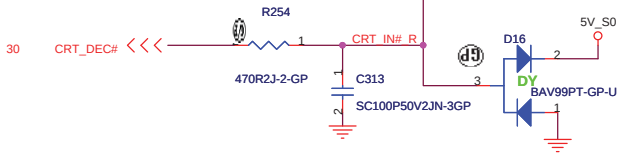
Hsync & Vsync level shift



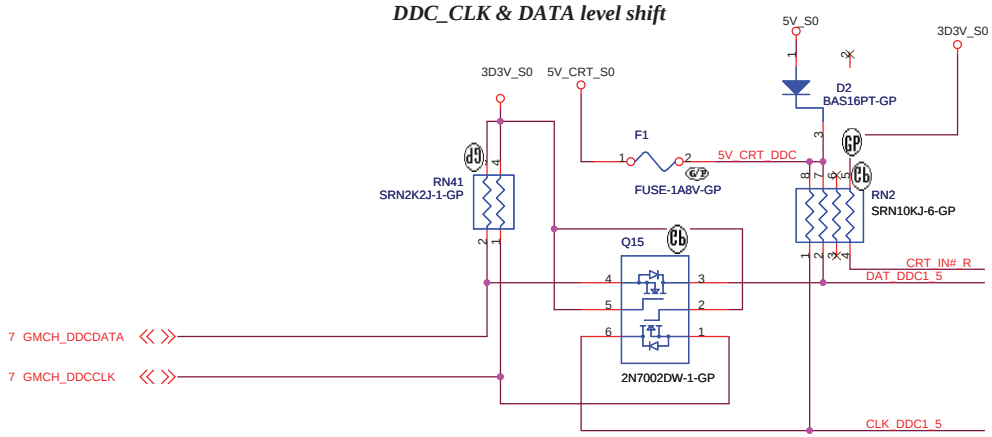
CRT I/F & CONNECTOR





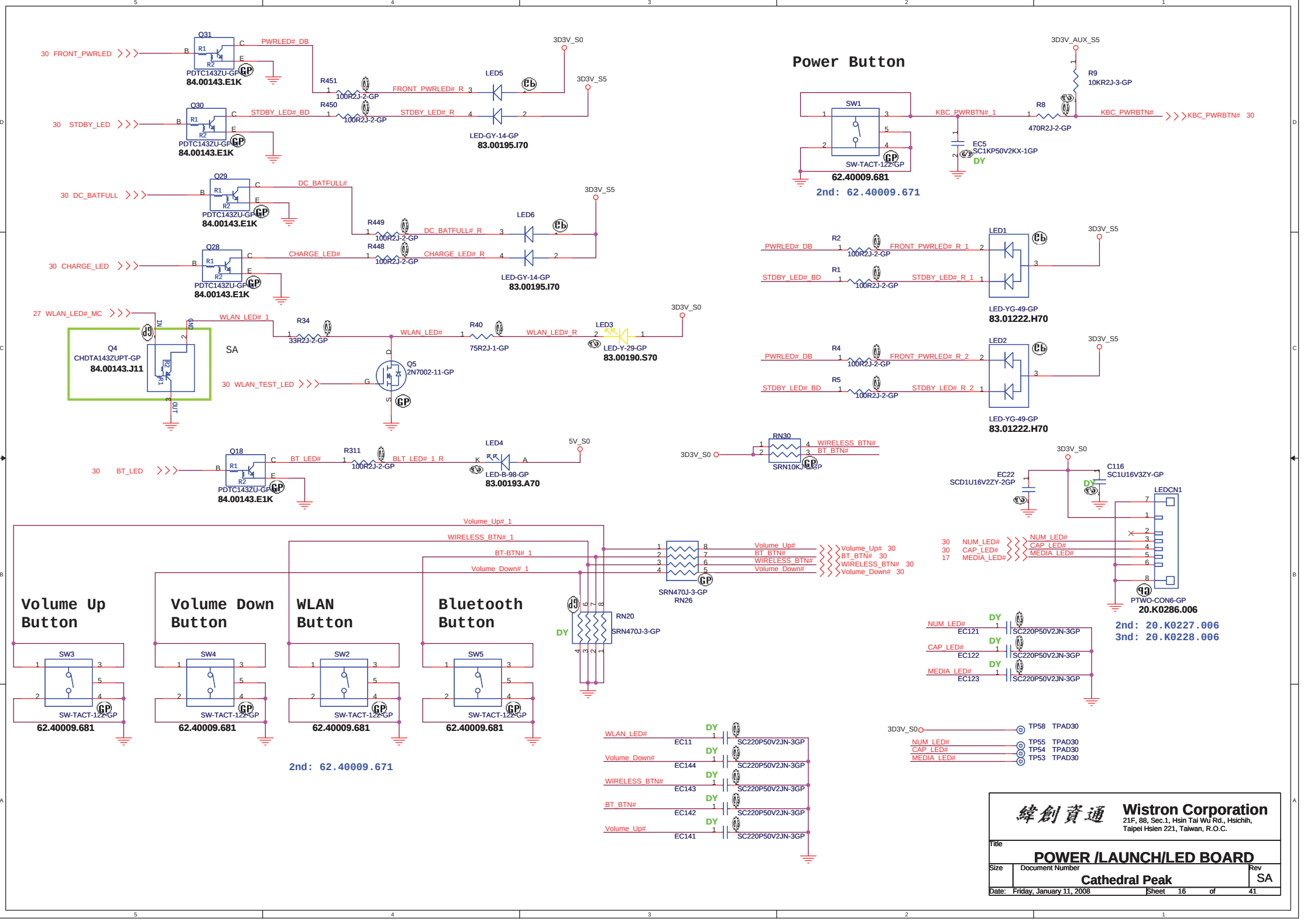


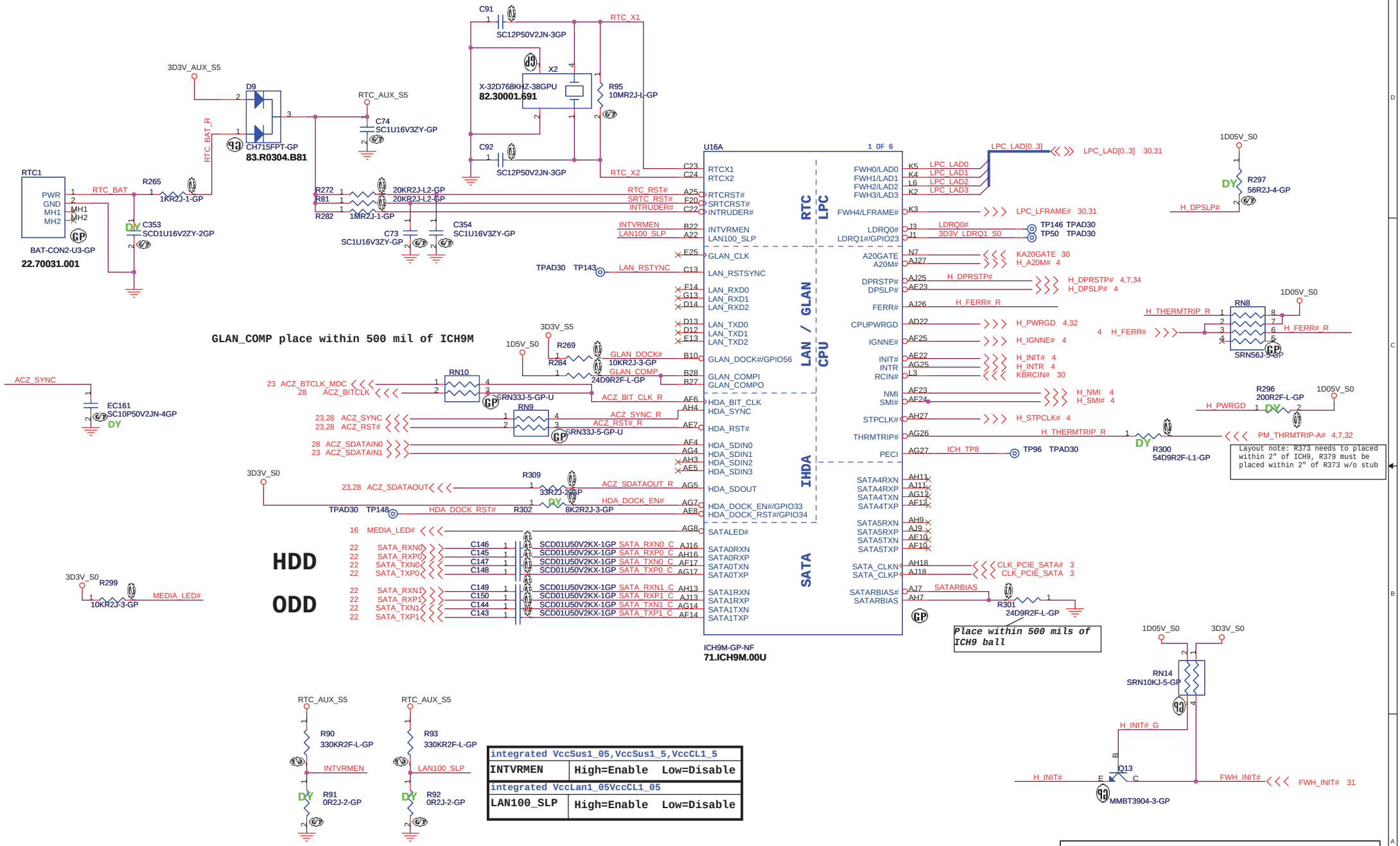
DDC_CLK & DATA level shift



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	CRT Connector	
Size	Document Number	Rev
	Cathedral Peak	SA
Date: Friday, January 11, 2008	Sheet 15 of 41	


Power Button
30 FRONT_PWRLED
30 STDBY_LED
30 DC_BATFULL
30 CHARGE_LED
27 WLAN_LED#_MC
30 BT_LED
30 WLAN_TEST_LED
Q31
Q30
Q29
Q28
Q18
Q4
CHDTA143ZUPT-GP
84.00143.J11
SA
Q5
2N7002-11-GP
PDTC143ZU-GP
84.00143.E1K
PWRLED# DB
STDBY_LED# BD
DC_BATFULL#
CHARGE_LED#
WLAN_LED# 1
WLAN_LED#
WLAN_LED# R
BT_LED#
BT_LED# 1 R
R451
R450
R449
R448
R34
R40
R311
100R2J-2-GP
33R2J-2-GP
75R2J-1-GP
FRONT_PWRLED# R
STDBY_LED# R
DC_BATFULL# R
CHARGE_LED# R
LED5
LED6
LED3
LED4
LED-GY-14-GP
83.00195.I70
LED-Y-29-GP
83.00190.S70
LED-B-98-GP
83.00193.A70
3D3V_S0
3D3V_S5
5V_S0
3D3V_AUX_S5
SW1
SW-TACT-122-GP
62.40009.681
2nd: 62.40009.671
KBC_PWRBTN# 1
KBC_PWRBTN#
KBC_PWRBTN# 30
R9
10KR2J-3-GP
R8
470R2J-2-GP
EC5
SC1KP50V2KX-1GP
DY
LED1
LED2
LED-YG-49-GP
83.01222.H70
FRONT_PWRLED# R 1
STDBY_LED# R 1
FRONT_PWRLED# R 2
STDBY_LED# R 2
R2
R1
R4
R5
RN30
SRN10KJ-3-GP
WIRELESS_BTN#
BT_BTN#
EC22
SCD1U16V2ZY-2GP
C116
SC1U16V3ZY-GP
LEDCN1
PTWO-CON6-GP
20.K0286.006
2nd: 20.K0227.006
3nd: 20.K0228.006
NUM_LED#
CAP_LED#
MEDIA_LED#
30 NUM_LED#
30 CAP_LED#
17 MEDIA_LED#
EC121
EC122
EC123
SC220P50V2JN-3GP
Volume_Up# 1
WIRELESS_BTN# 1
BT-BTN# 1
Volume_Down# 1
Volume_Up#
BT_BTN#
WIRELESS_BTN#
Volume_Down#
Volume_Up# 30
BT_BTN# 30
WIRELESS_BTN# 30
Volume_Down# 30
SRN470J-3-GP
RN26
RN20
Volume Up Button
Volume Down Button
WLAN Button
Bluetooth Button
SW3
SW4
SW2
SW5
EC11
EC144
EC143
EC142
EC141
TP58 TPAD30
TP55 TPAD30
TP54 TPAD30
TP53 TPAD30
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER /LAUNCH/LED BOARD
Size
Document Number
Cathedral Peak
Rev
SA
Date: Friday, January 11, 2008
Sheet 16 of 41



Wistron Corporation
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Title: ICH9-M (1 of 4)

Size | Document Number: Cathedral Peak | Rev: SA

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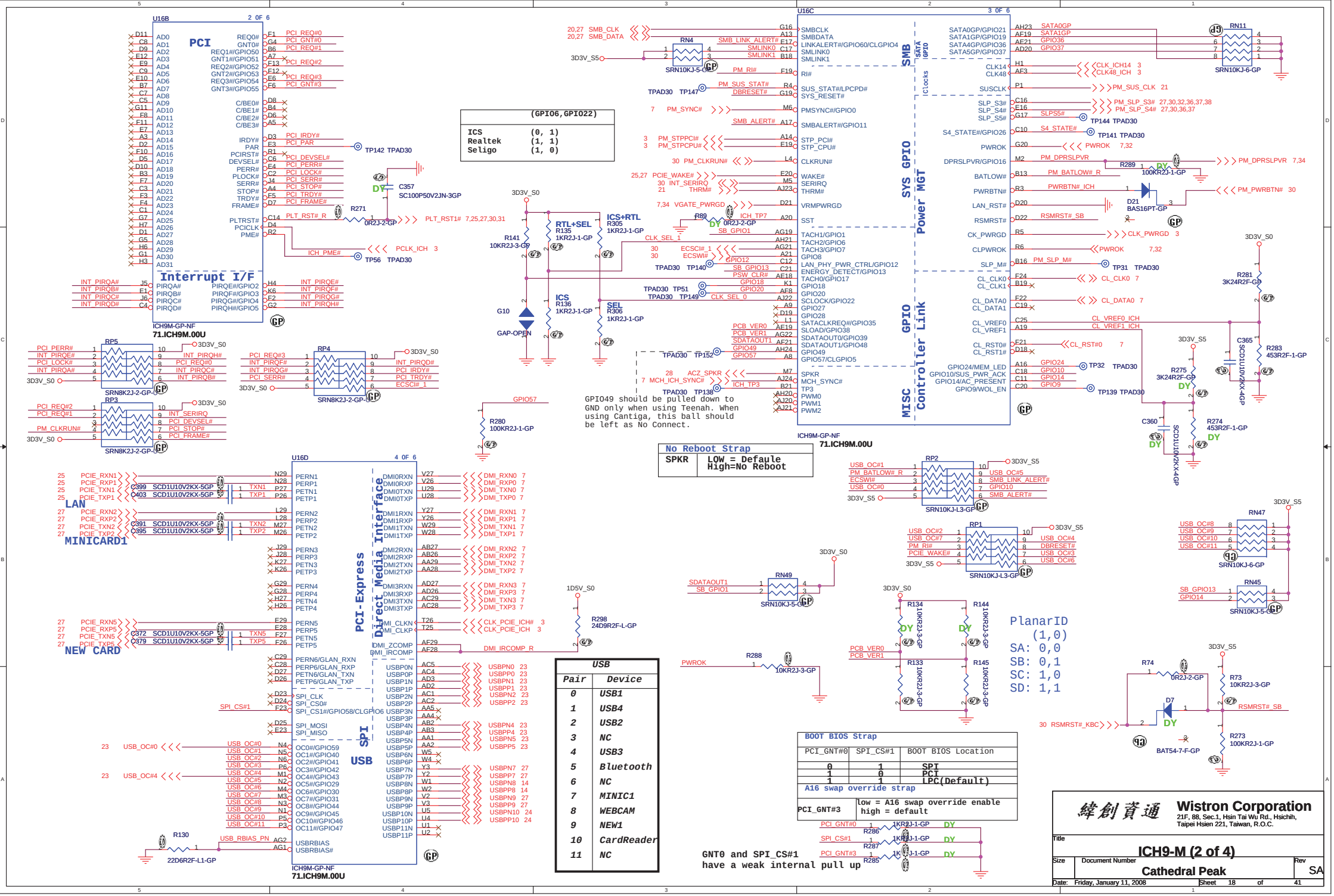
U16B
2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
U16C
3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
U16D
4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
LAN
MINICARD1
NEW CARD
(GPIO6,GPIO22)
ICS (0, 1)
Realtek (1, 1)
Seligo (1, 0)
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR LOW = Defaule
High=No Reboot
USB
Pair Device
0 USB1
1 USB4
2 USB2
3 NC
4 USB3
5 Bluetooth
6 NC
7 MINIC1
8 WEBCAM
9 NEW1
10 CardReader
11 NC
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
GNT0 and SPI_CS#1 have a weak internal pull up
Wistron Corporation
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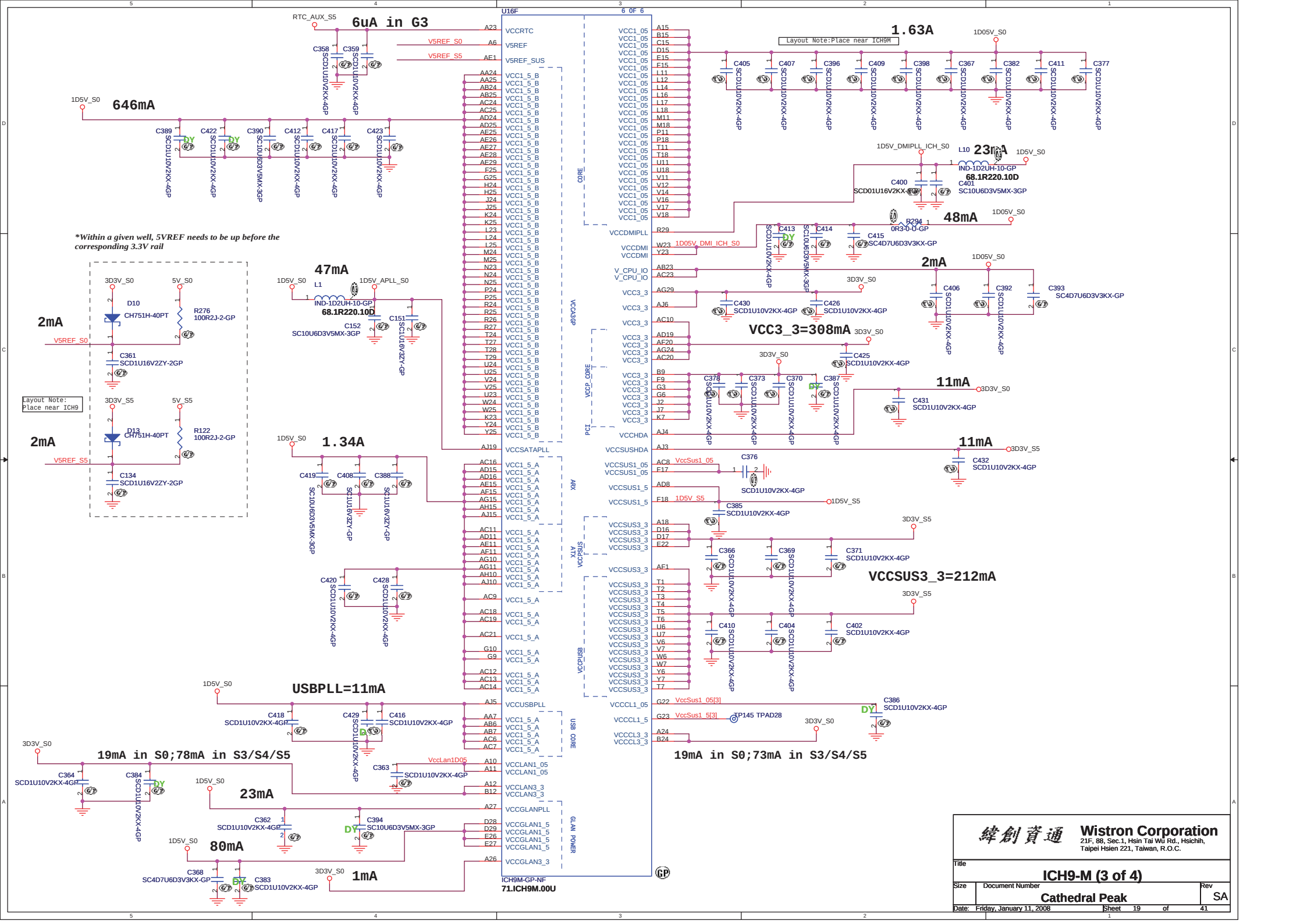
Title
ICH9-M (2 of 4)
Size
Document Number
Cathedral Peak
Rev
SA
Date: Friday, January 11, 2008
Sheet 18 of 41


U16F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
6uA in G3
646mA
1.63A
Layout Note:Place near ICH9M
23mA
68.1R220.10D
48mA
2mA
47mA
68.1R220.10D
VCC3_3=308mA
11mA
11mA
1.34A
2mA
2mA
Layout Note: Place near ICH9
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
USBPLL=11mA
VCCSUS3_3=212mA
19mA in S0;78mA in S3/S4/S5
19mA in S0;73mA in S3/S4/S5
23mA
80mA
1mA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 4)
Size
Document Number
Cathedral Peak
Rev
SA
Date: Friday, January 11, 2008
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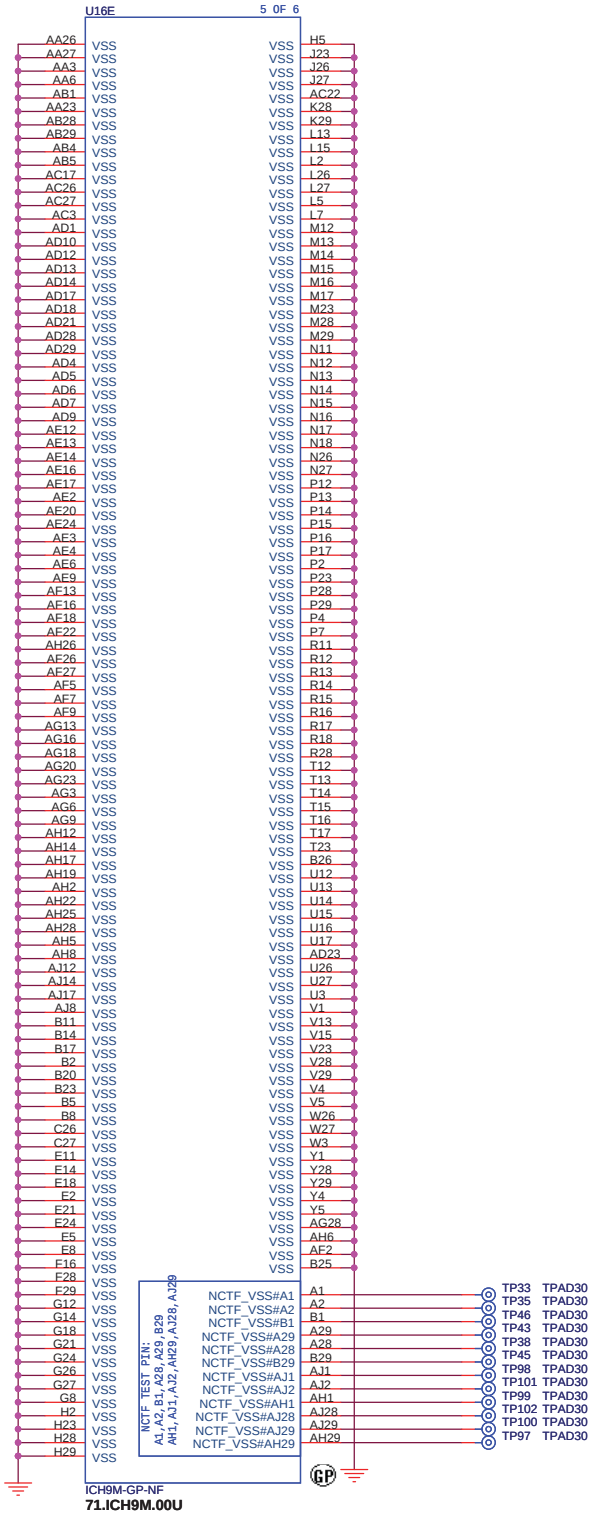

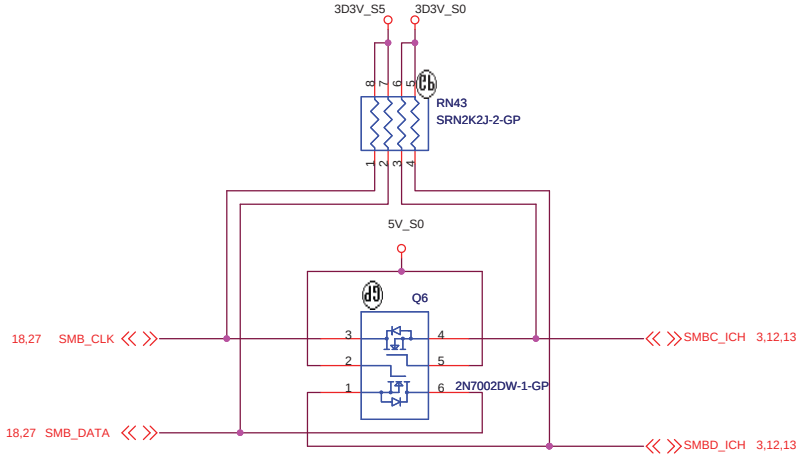

SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (4 of 4)

Size | Document Number: Cathedral Peak | Rev: SA

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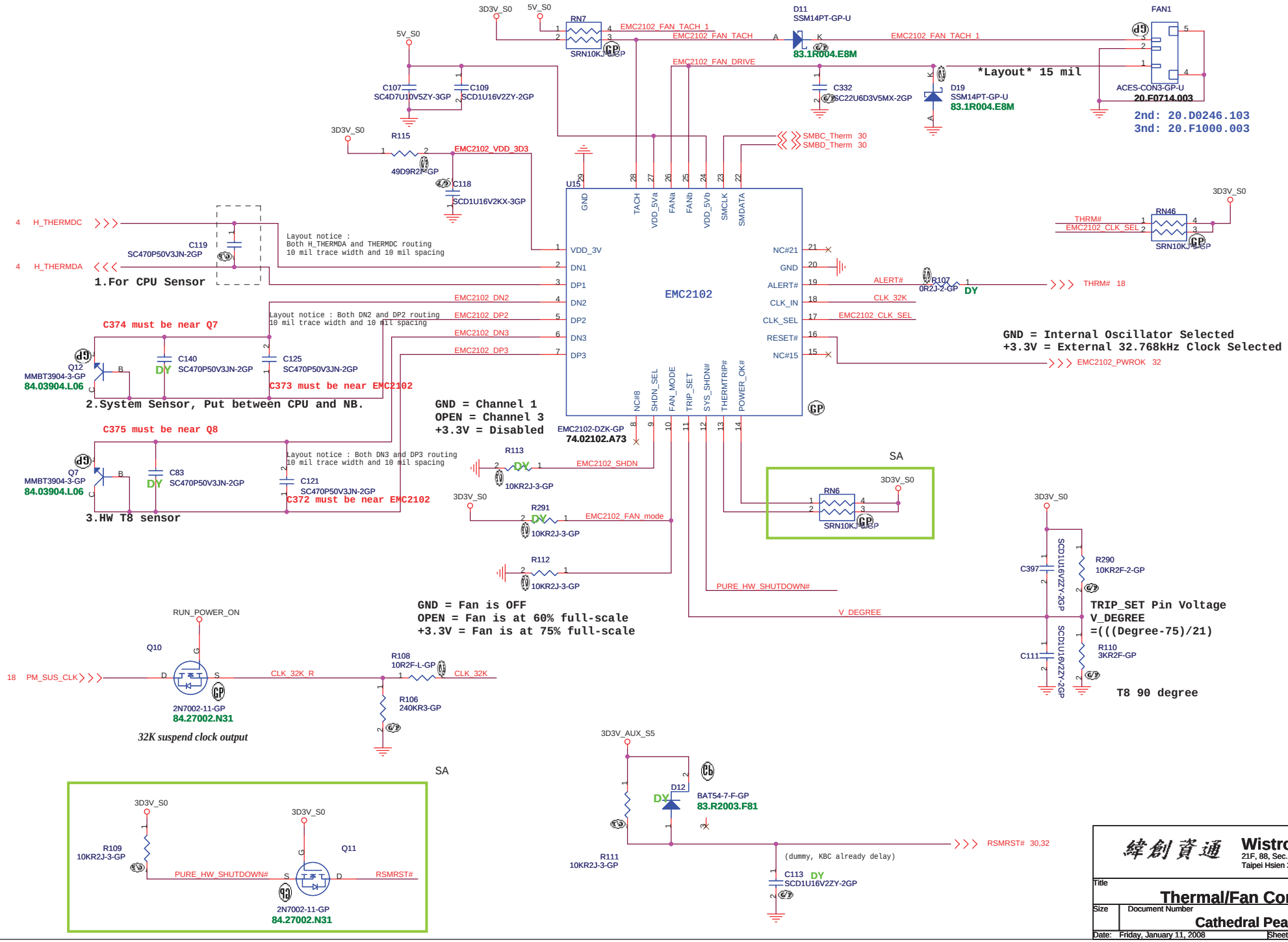

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Thermal/Fan Controllor	
Size	Document Number: Cathedral Peak	Rev: SA
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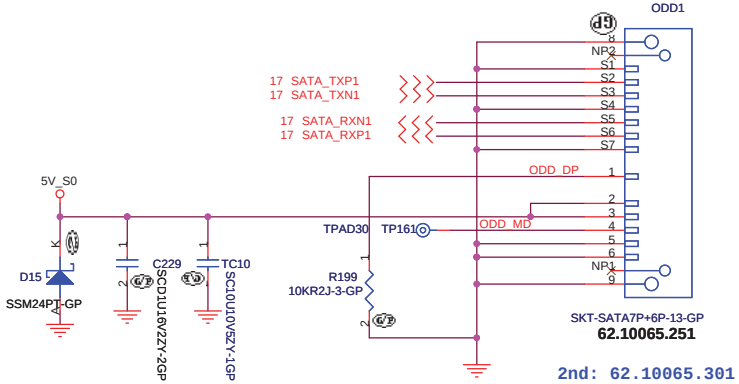
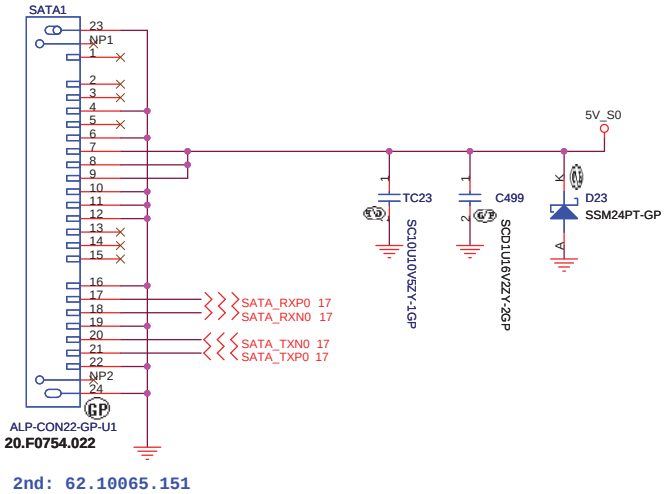
SATA ODD Connector



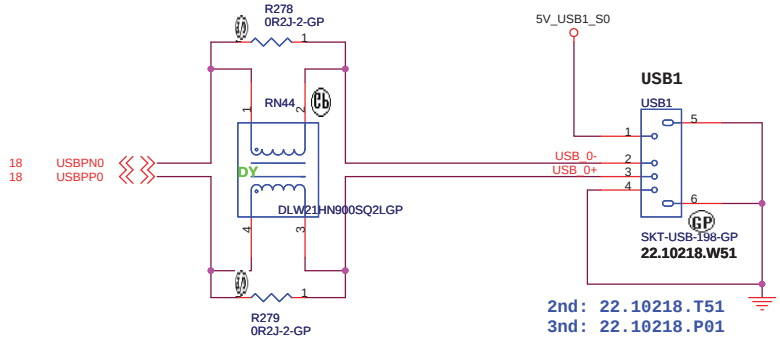
SATA Connector

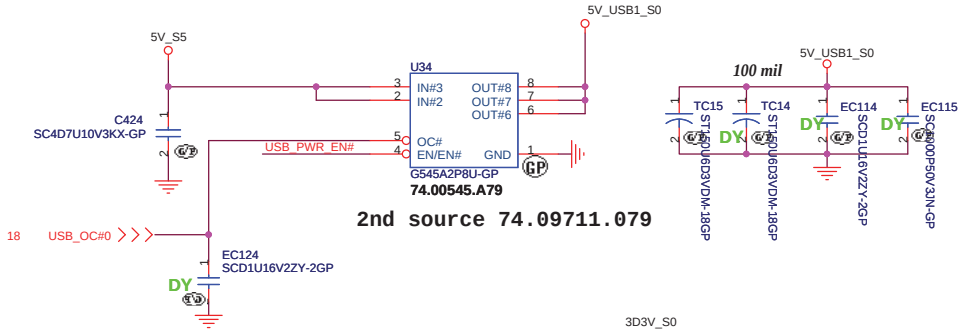


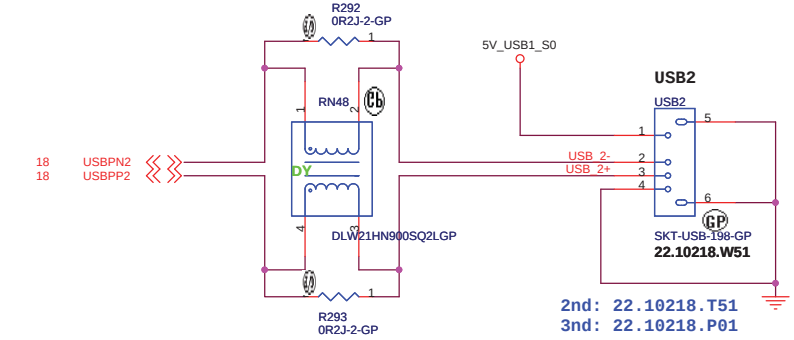
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD & CDROM		
Size	Document Number: Cathedral Peak	Rev: SA
Date: Friday, January 11, 2008	Sheet 22 of 41	

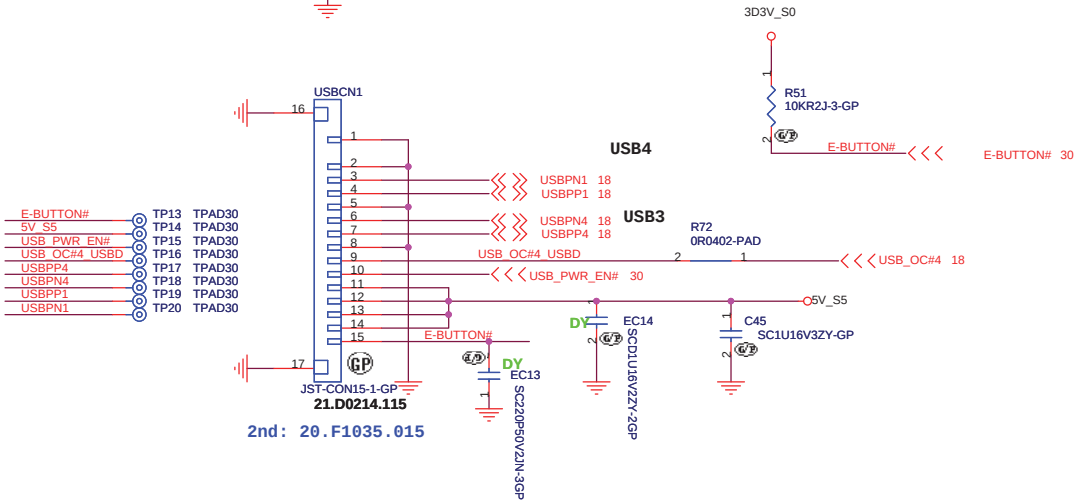
Co-Layout Common Mode Choke and 0 Ohm





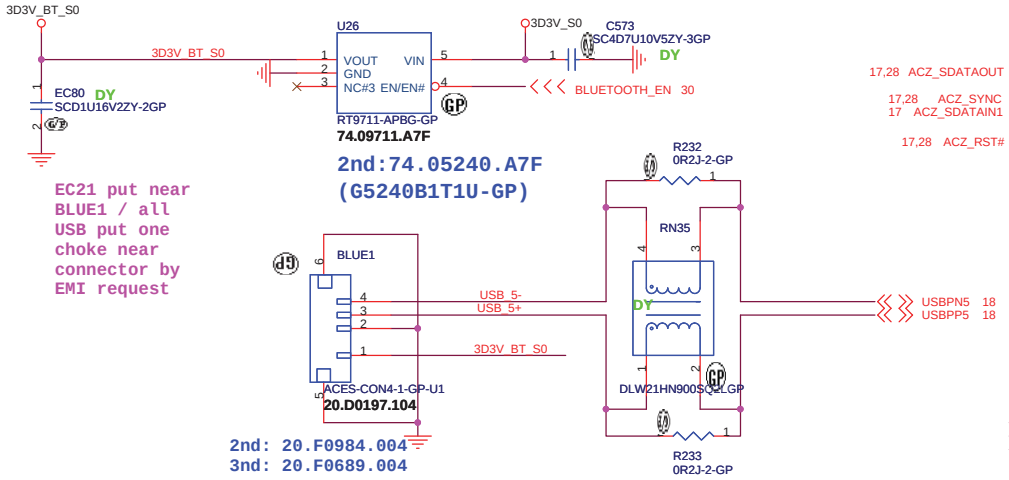


Co-Layout Common Mode Choke and 0 Ohm

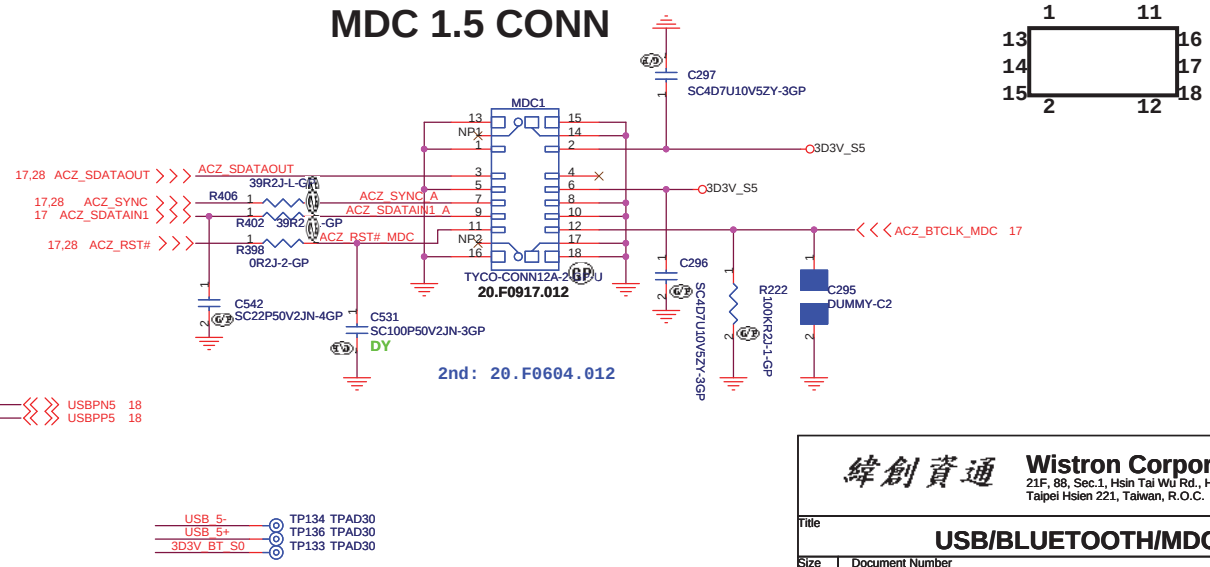


BLUETOOTH MODULE

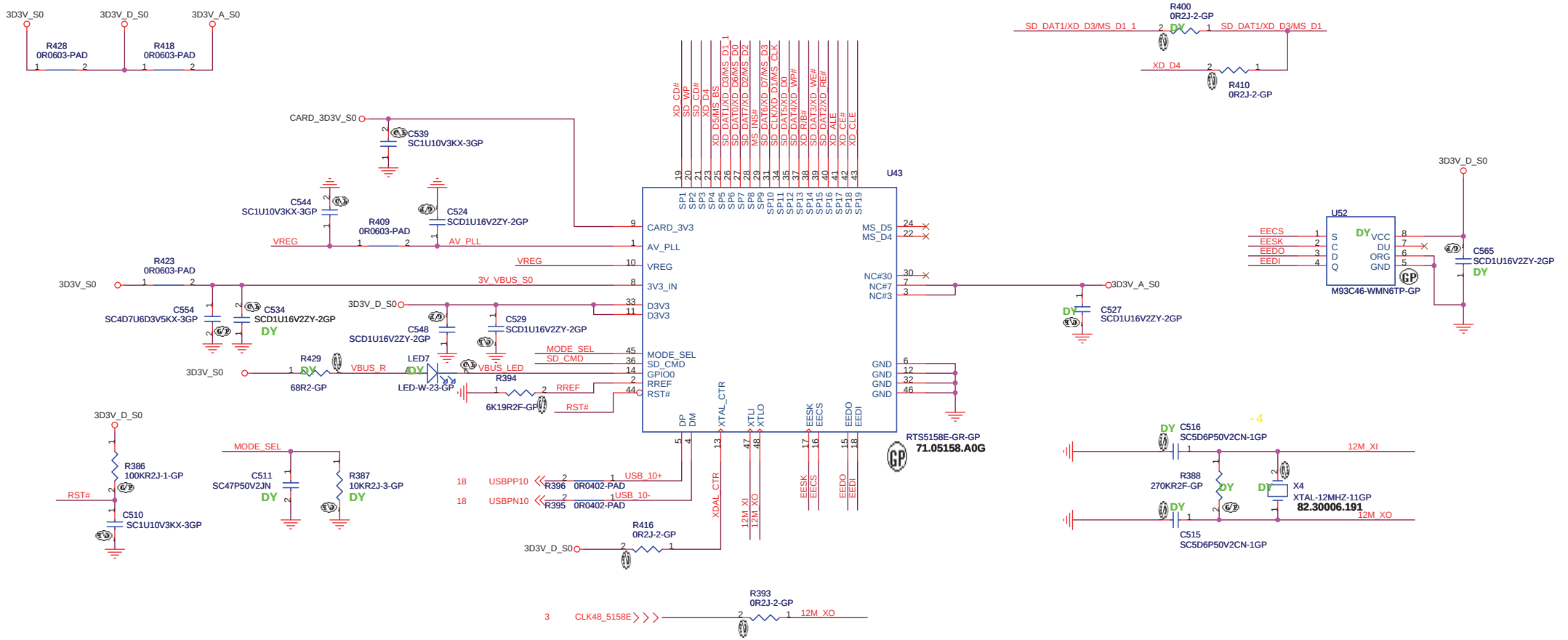
1.5A / High Active Voltage 2V



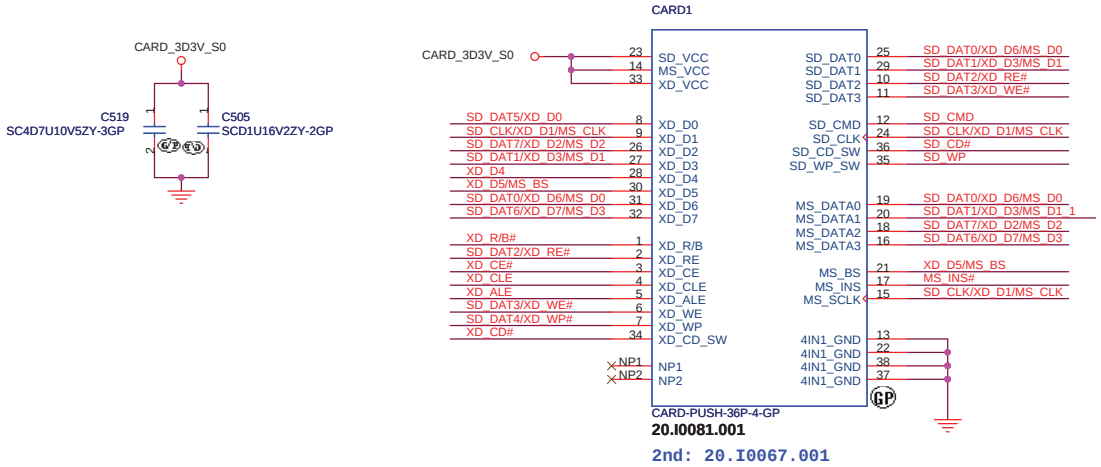
MDC 1.5 CONN



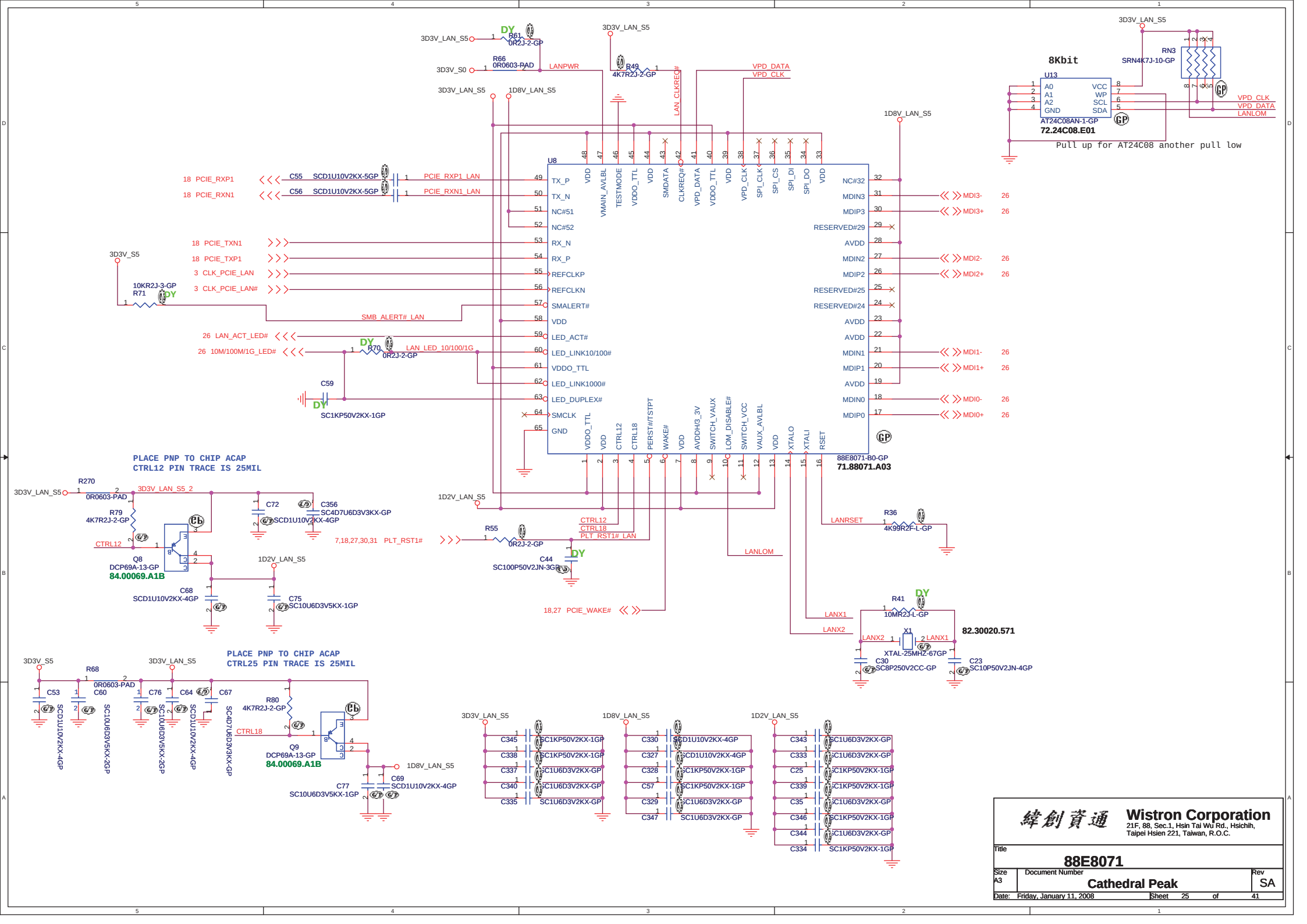
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	USB/BLUETOOTH/MDC	
Size	Document Number: Cathedral Peak	Rev: SA
Date: Friday, January 11, 2008	Sheet 23 of 41	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CARDREADER- RTS5158E**	
Size	Document Number: **Cathedral Peak**	Rev: SA
Date: Friday, January 11, 2008	Sheet 24 of 41	


U8
88E8071-B0-GP
71.88071.A03
TX_P
TX_N
NC#51
NC#52
RX_N
RX_P
REFCLKP
REFCLKN
SMALERT#
VDD
LED_ACT#
LED_LINK10/100#
VDDO_TTL
LED_LINK1000#
LED_DUPLEX#
SMCLK
GND
NC#32
MDIN3
MDIP3
RESERVED#29
AVDD
MDIN2
MDIP2
RESERVED#25
RESERVED#24
MDIN1
MDIP1
MDIN0
MDIP0
VMAIN_AVLBL
TESTMODE
SMDATA
CLKREQ#
VPD_DATA
VPD_CLK
SPI_CLK
SPI_CS
SPI_DI
SPI_DO
PERST#/TSTPT
WAKE#
AVDDH/3_3V
SWITCH_VAUX
LOM_DISABLE#
SWITCH_VCC
VAUX_AVLBL
XTALO
XTALI
RSET
PCIE_RXP1_LAN
PCIE_RXN1_LAN
LAN_CLKREQ#
LAN_LED_10/100/1G
PLT_RST1# LAN
LANPWR
LANRSET
LANLOM
LANX1
LANX2
SMB_ALERT# LAN
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
Q8
DCP69A-13-GP
84.00069.A1B
Q9
DCP69A-13-GP
84.00069.A1B
8Kbit
U13
AT24C08AN-1-GP
72.24C08.E01
Pull up for AT24C08 another pull low
RN3
SRN4K7J-10-GP
X1
XTAL-25MHZ-67GP
82.30020.571
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
88E8071
Size A3
Document Number
Cathedral Peak
Rev SA
Date: Friday, January 11, 2008
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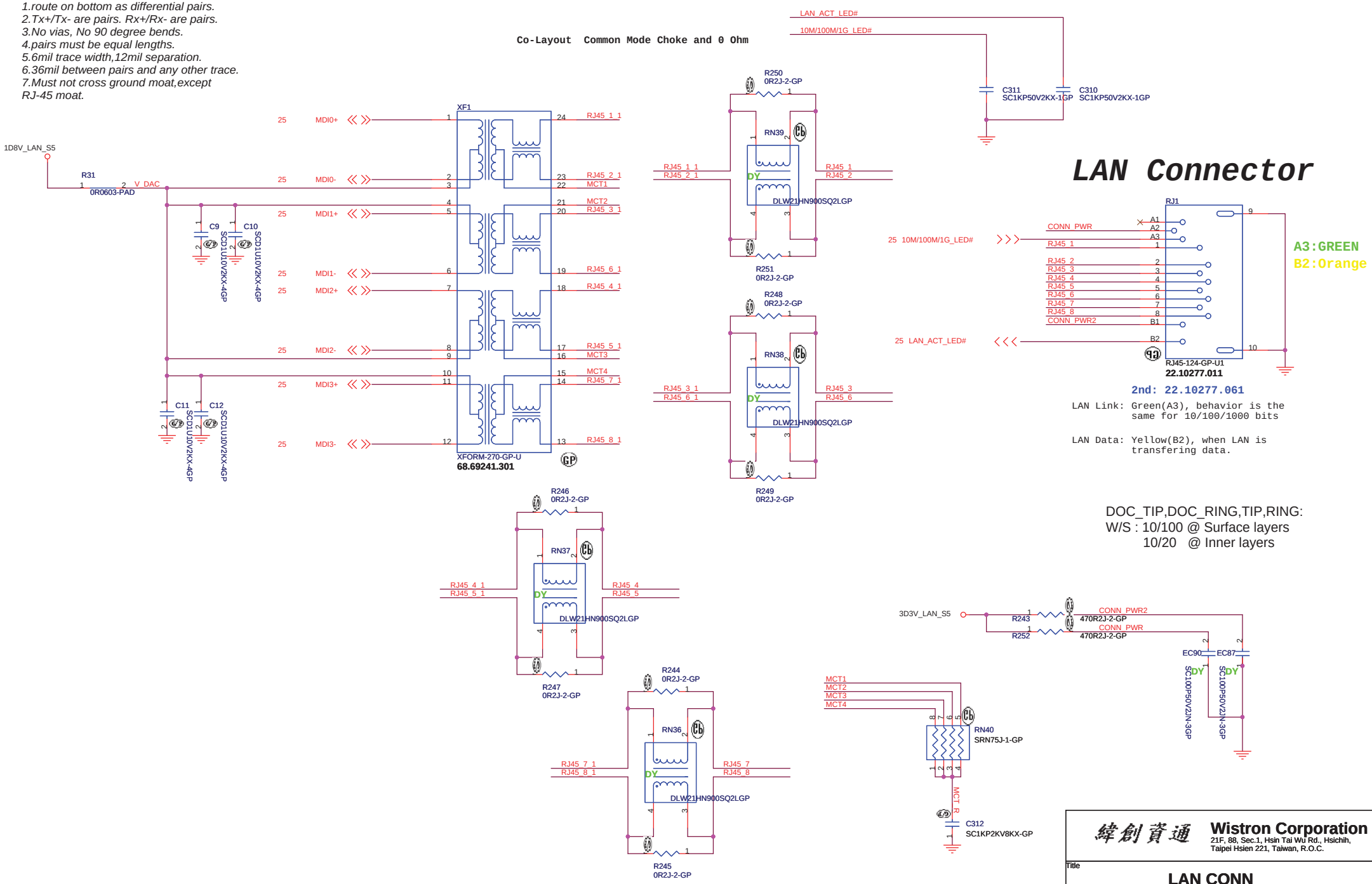
LAN Connector

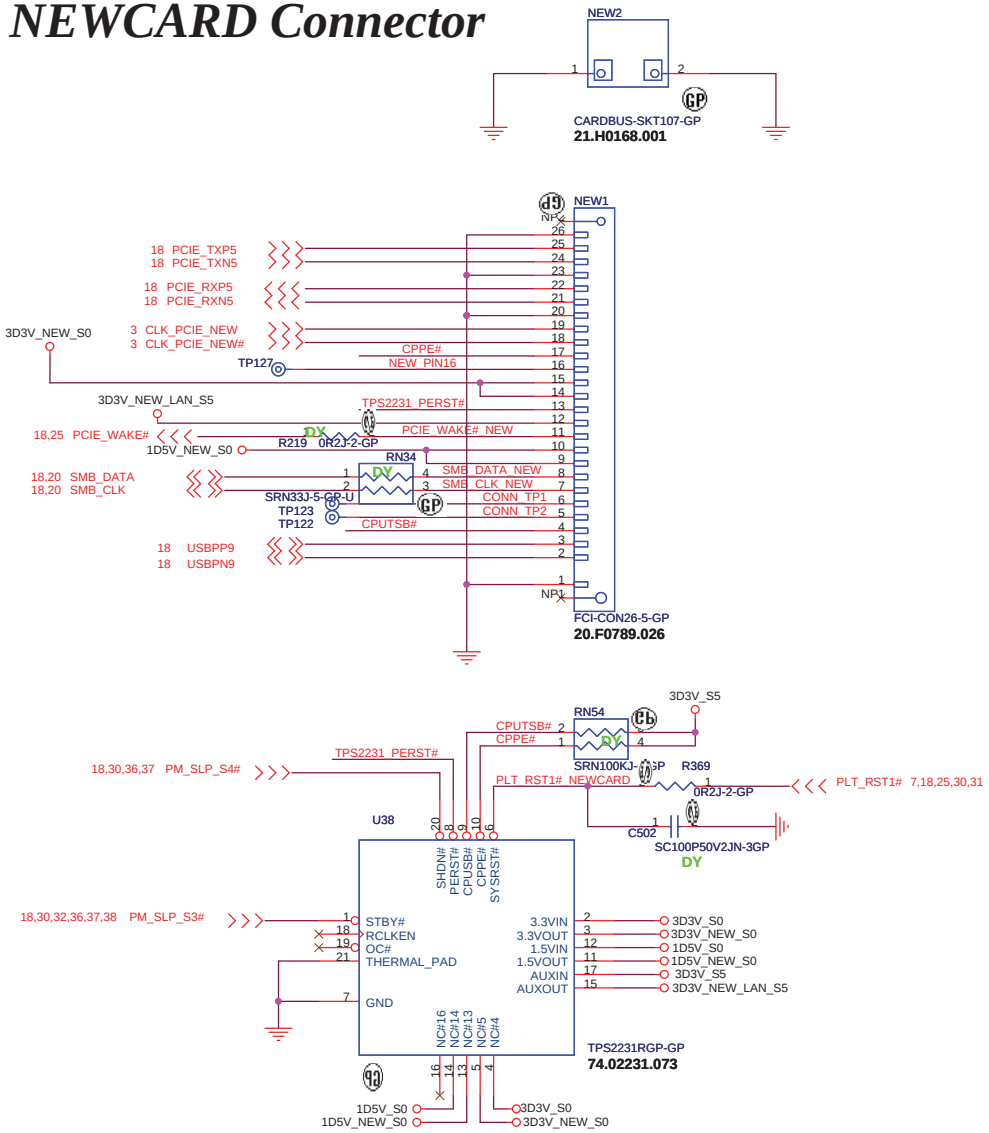
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

Co-Layout Common Mode Choke and 0 Ohm

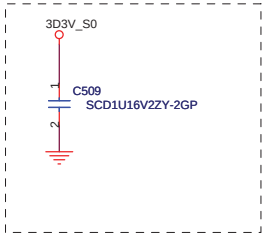


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN CONN	
Size A3	Document Number Cathedral Peak	Rev SA
Date: Friday, January 11, 2008	Sheet 26 of 41	

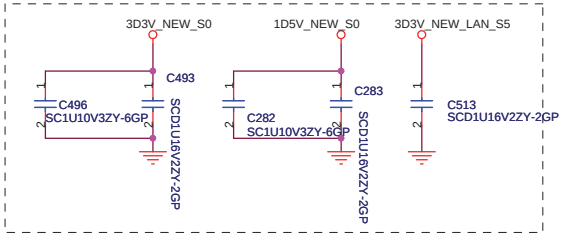
NEWCARD Connector



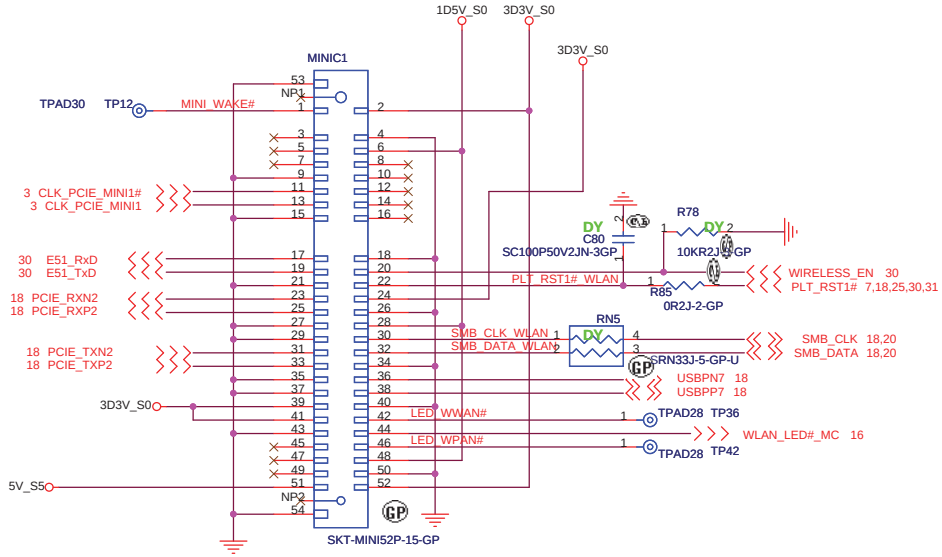
Place them Near to Chip



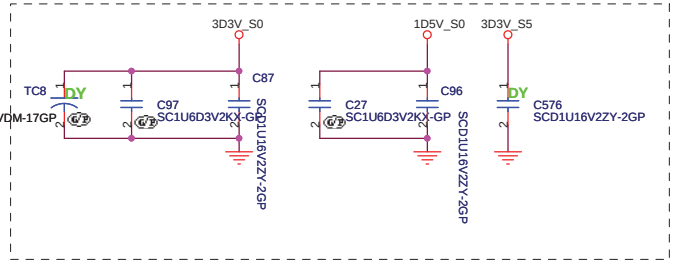
Place them Near to Connector



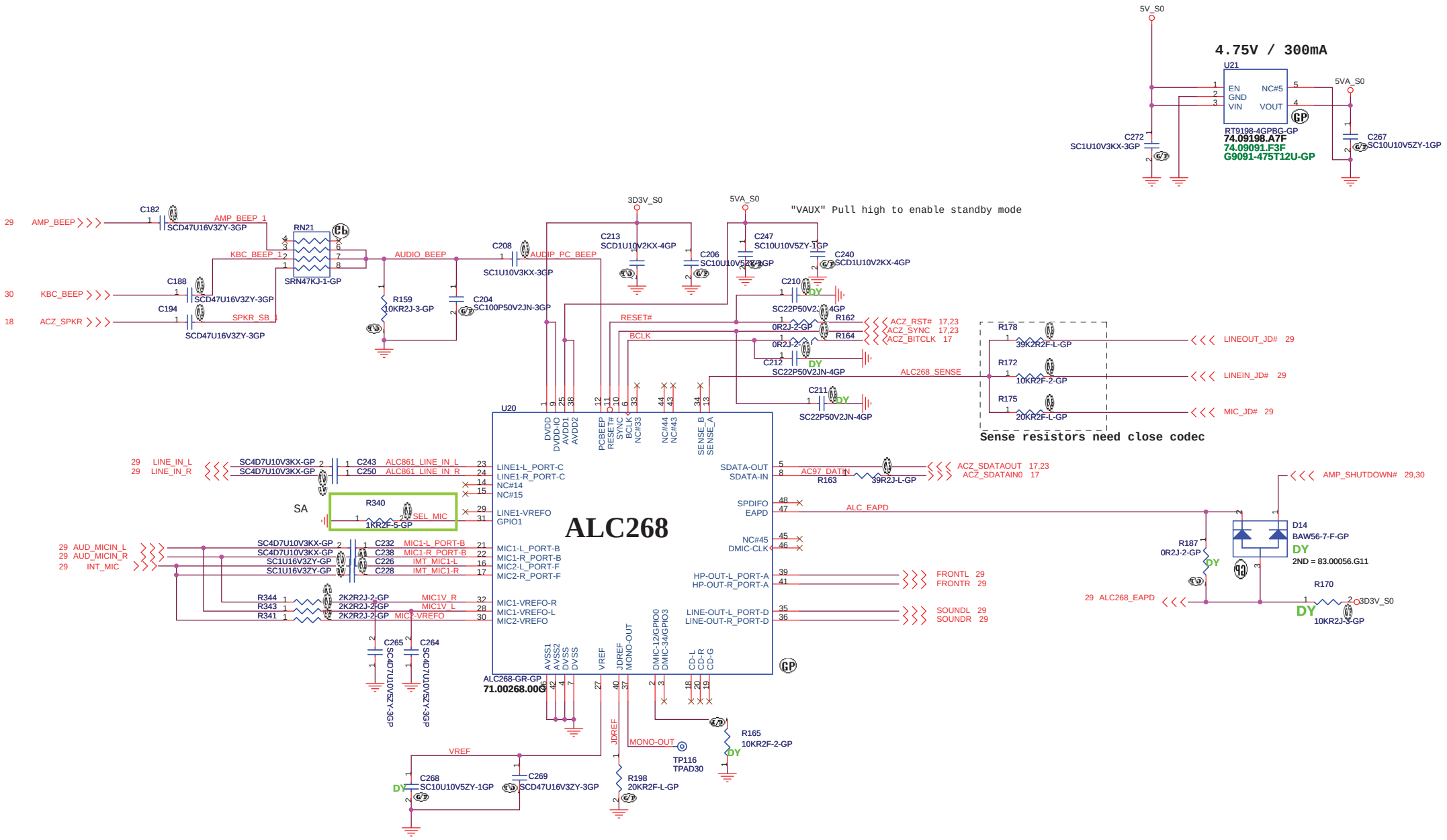
Mini Card Connector(WLAN)



Place near MINIC1



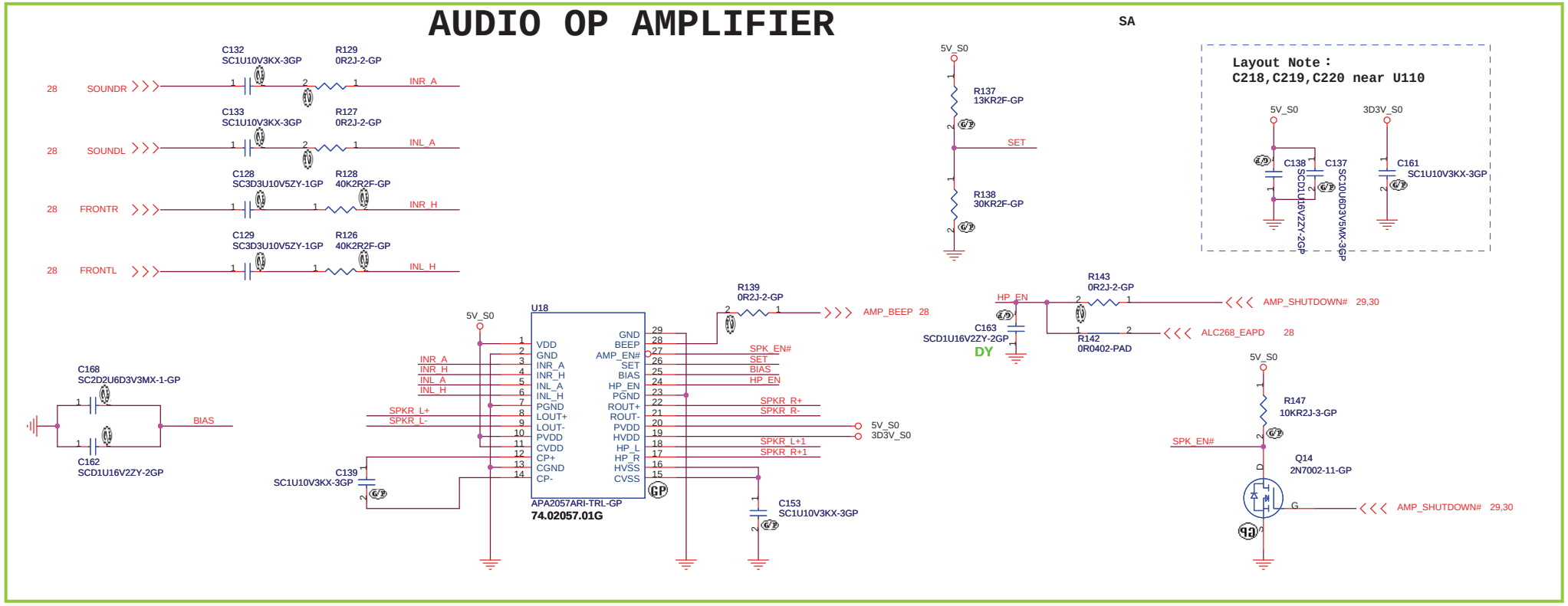
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**NEW CARD/MINI CARD**	
Size	Document Number **Cathedral Peak**	Rev SA
Date: Friday, January 11, 2008	Sheet 27 of 41	



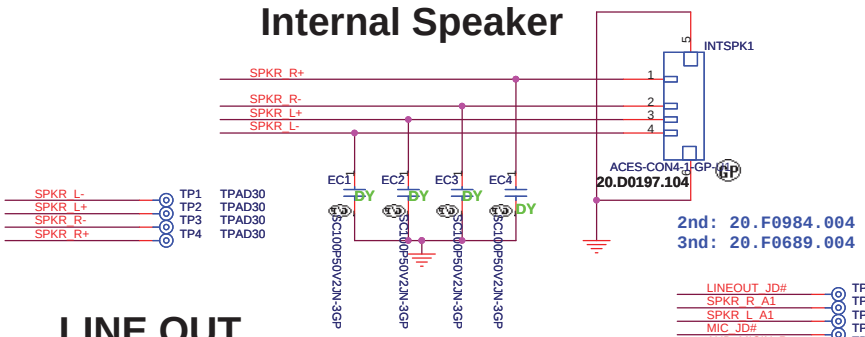
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Azalia codec ALC268**
Size A3	Document Number **Cathedral Peak** Rev SA
Date: Friday, January 11, 2008	Sheet 28 of 41

AUDIO OP AMPLIFIER

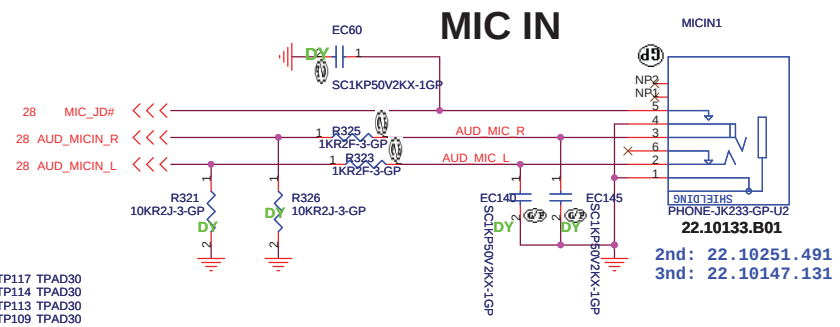
SA



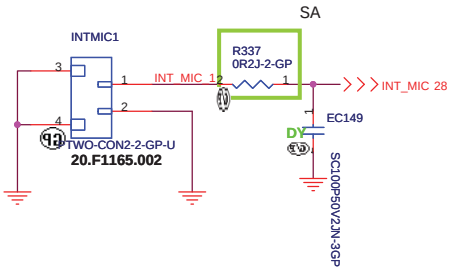
Internal Speaker



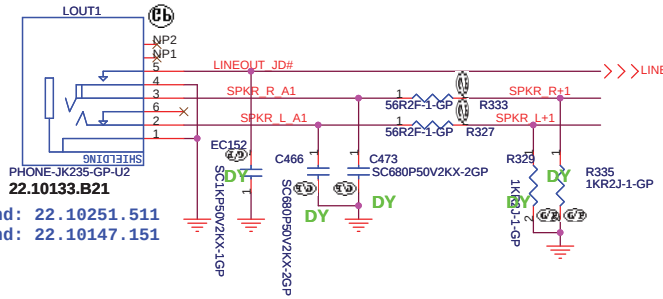
MIC IN

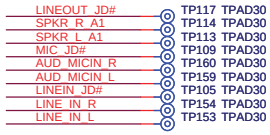


Analog Int. Mic

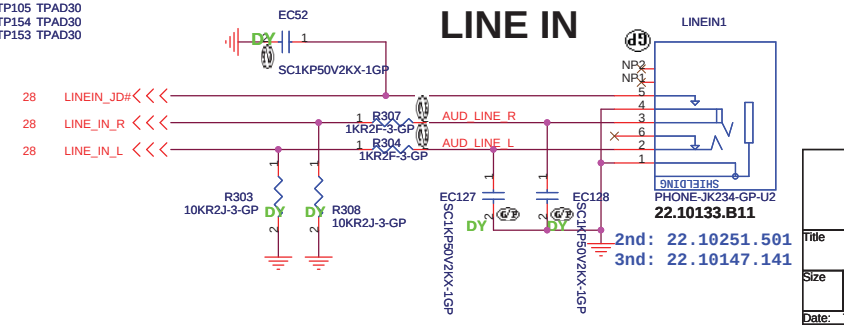


LINE OUT





LINE IN



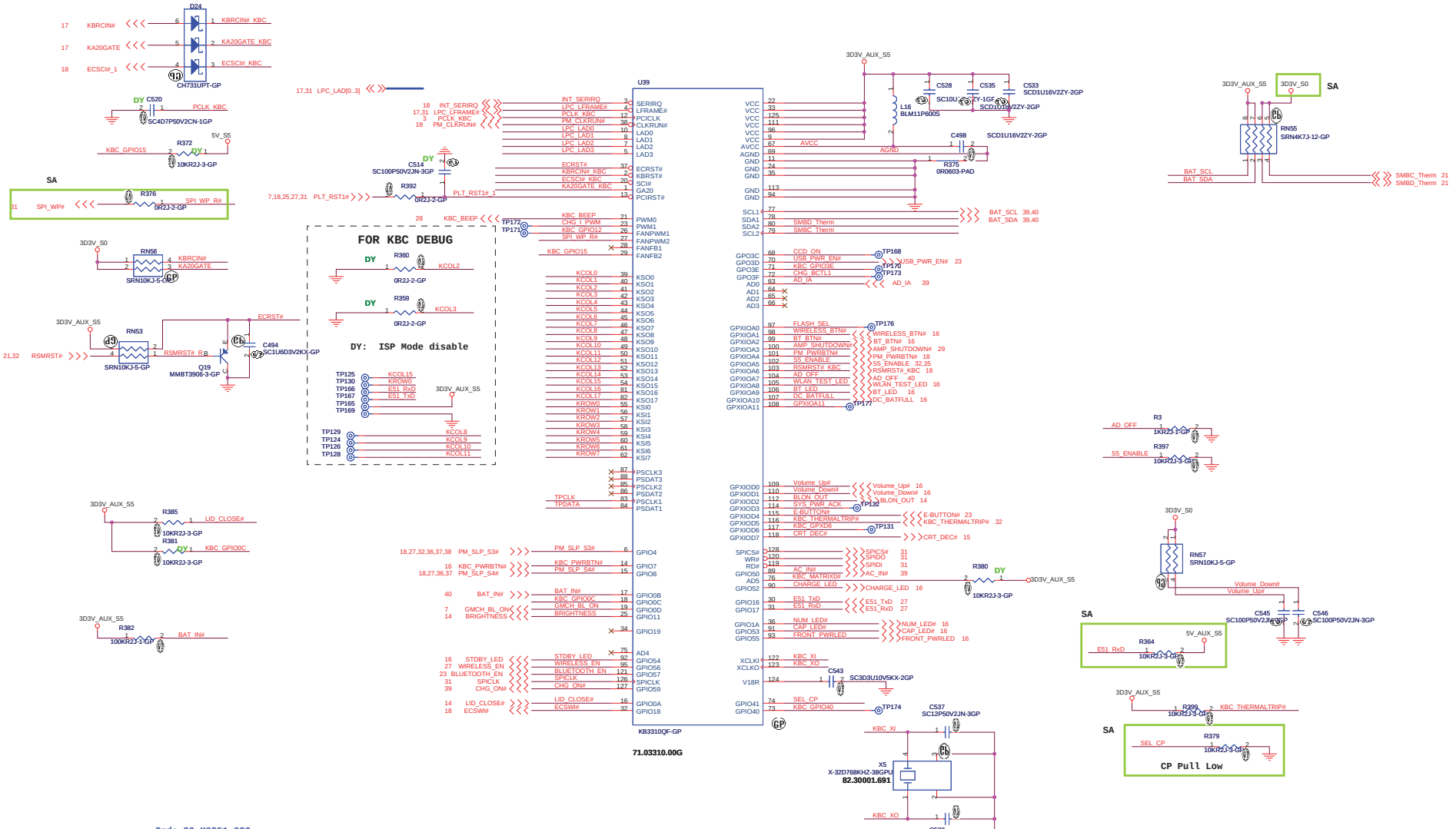
INT_MIC TP162 TPAD30

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK

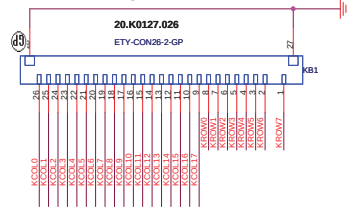
Size: | Document Number: Cathedral Peak | Rev: SA

Date: Tuesday, January 15, 2008 | Sheet 29 of 41

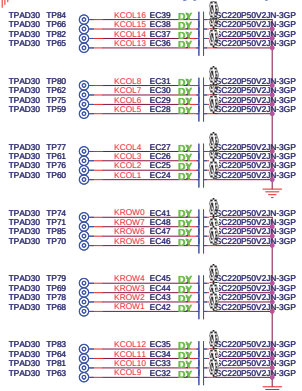


2nd: 20.K0251.026

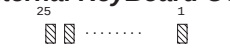
Internal KeyBoard Connector



EMI Bypass cap.

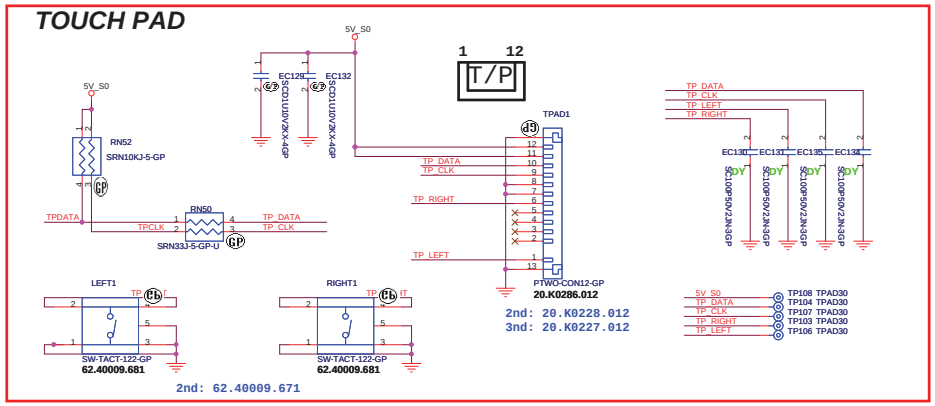


Internal KeyBoard CONN



CHECK KB SPEC. AND PIN DEFINE

TOUCH PAD



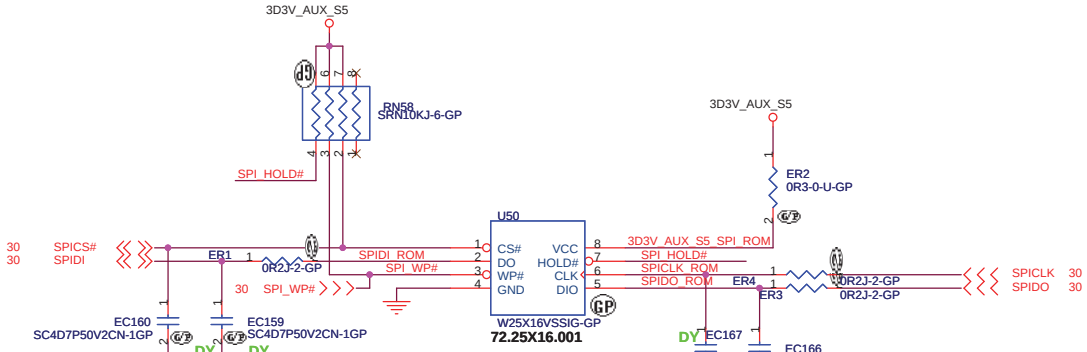
2nd: 20.K0228.012
3nd: 20.K0227.012
2nd: 62.40009.671

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC ENE3926

Size: A2 | Document Number: Cathedral Peak | Rev: SA

Date: Friday, January 11, 2008 | Sheet 30 of 41



16M Bits SPI FLASH ROM

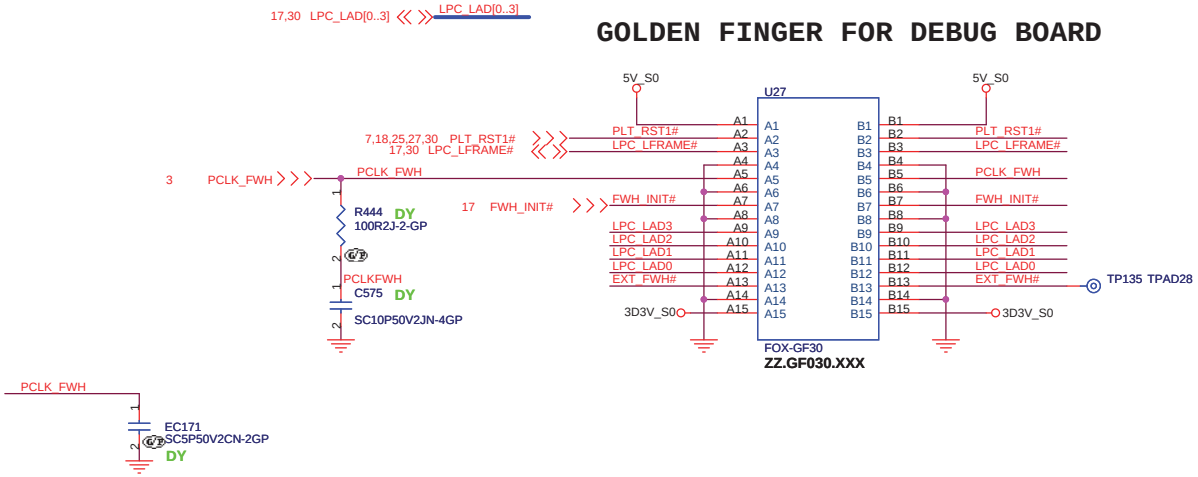
MXIC: 72.25165.001
WinBond: 72.25X16.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

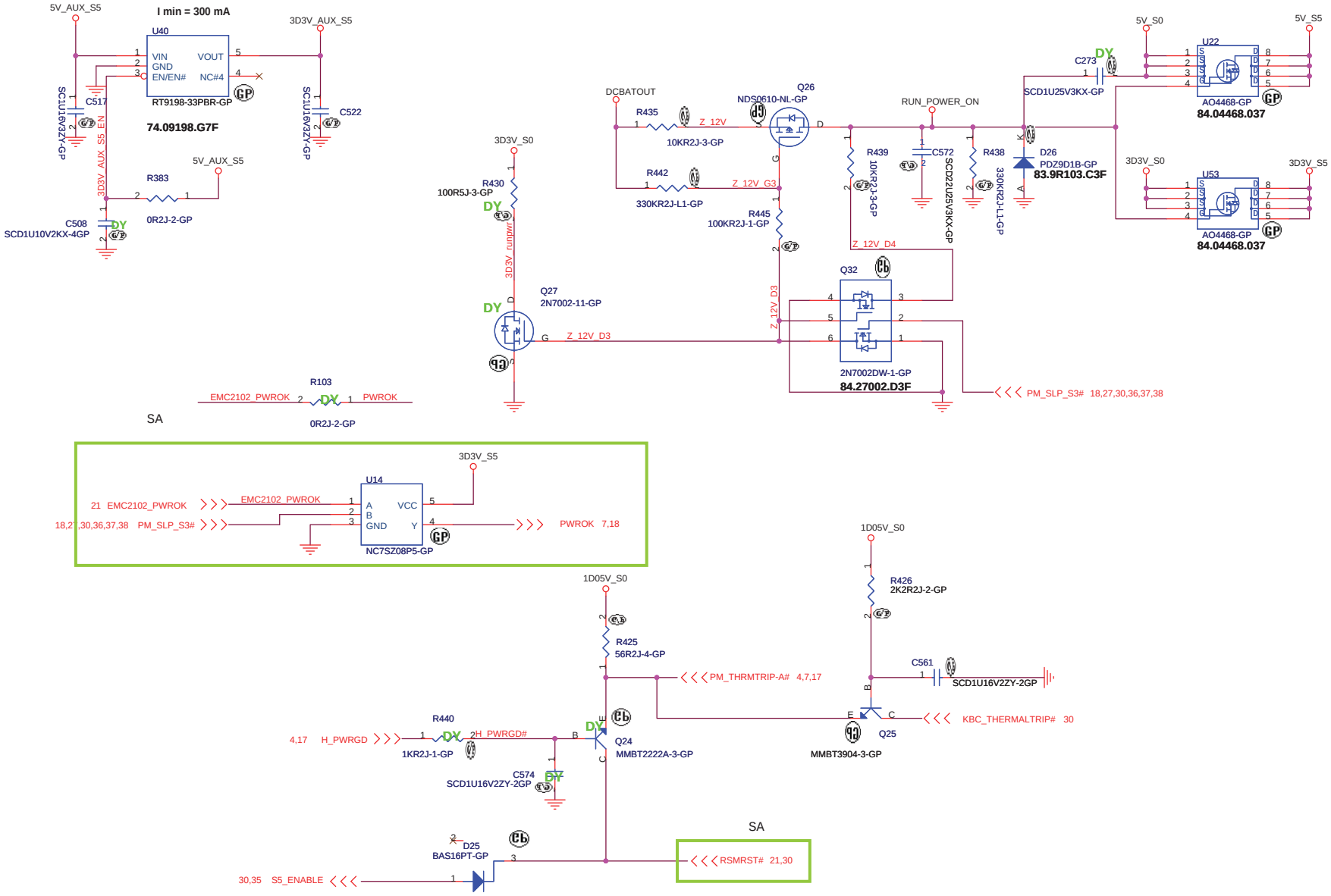


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

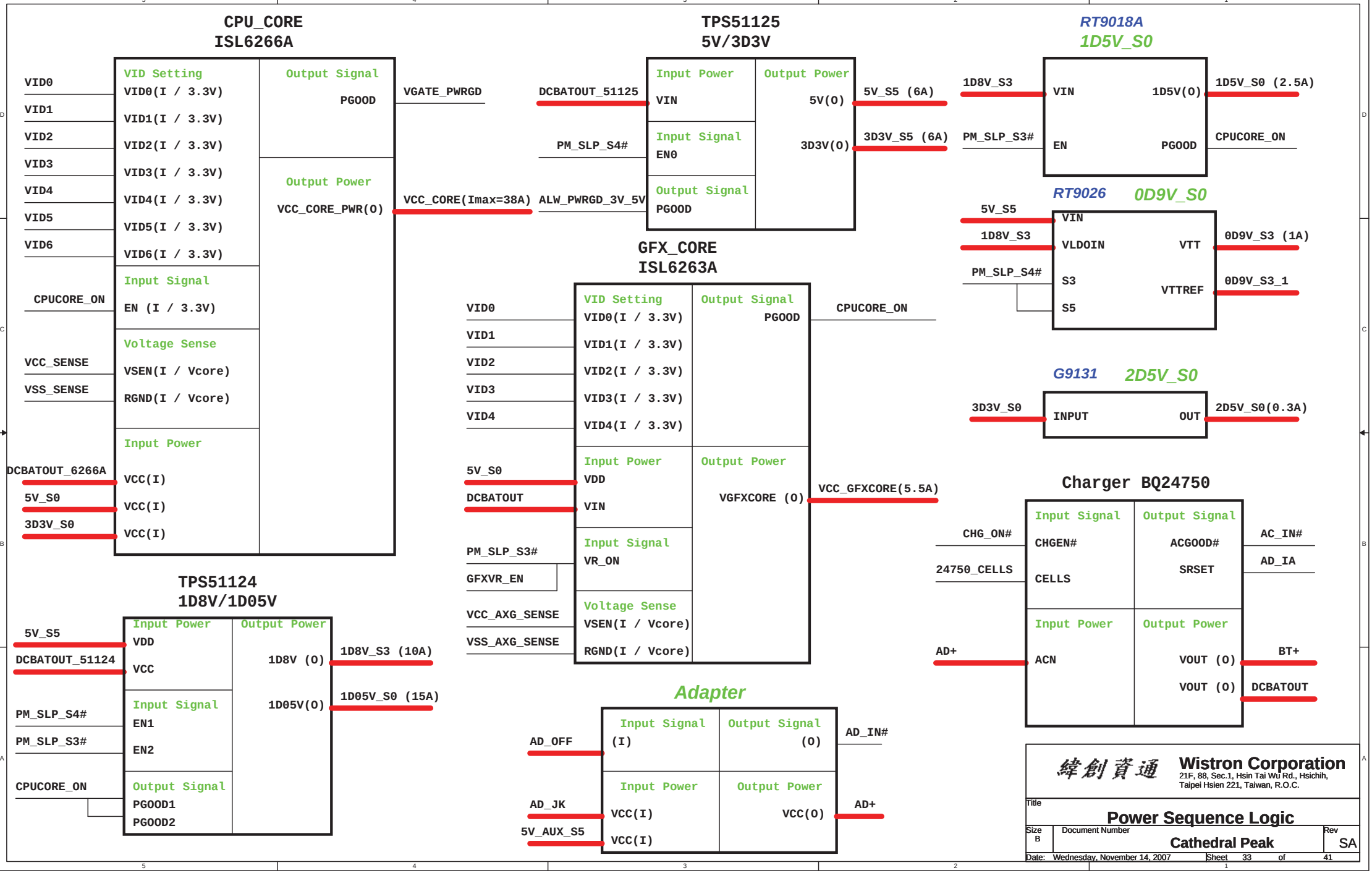
Title	BIOS/GOLDEN FINGER	
Size	Document Number: Cathedral Peak	Rev: SA
Date: Friday, January 11, 2008	Sheet 31 of 41	

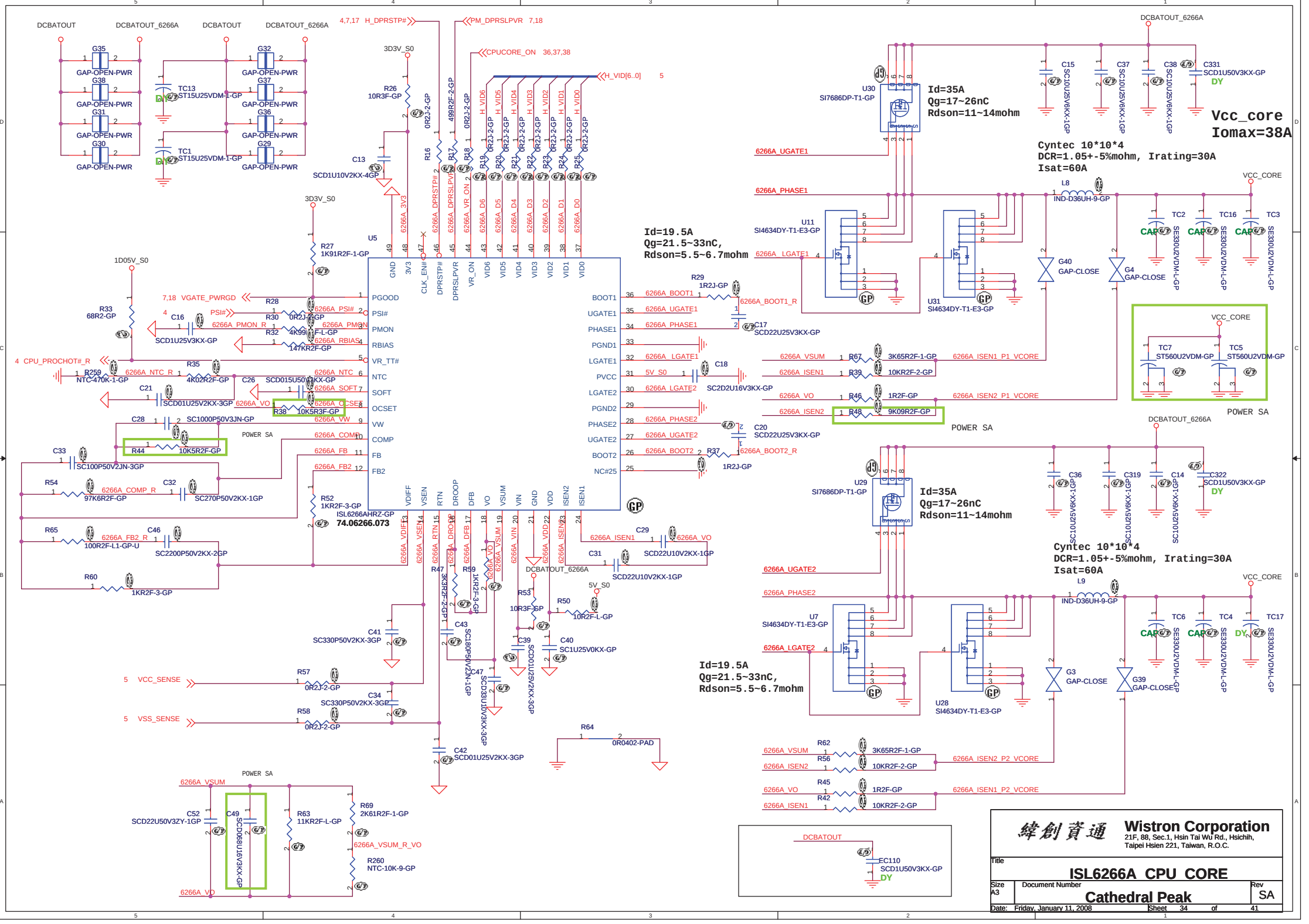
Aux Power 3D3V_AUX_S5

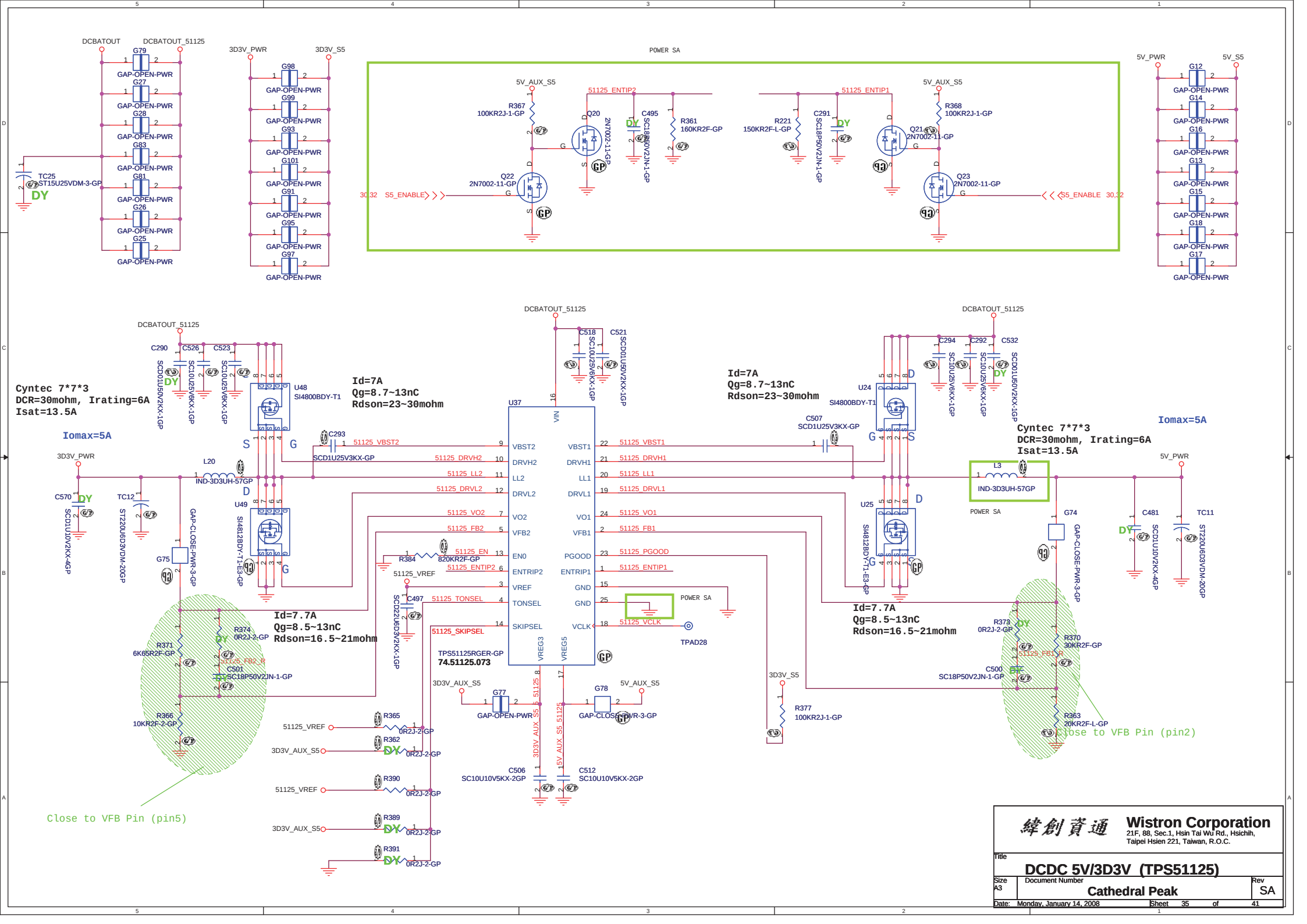
Run Power

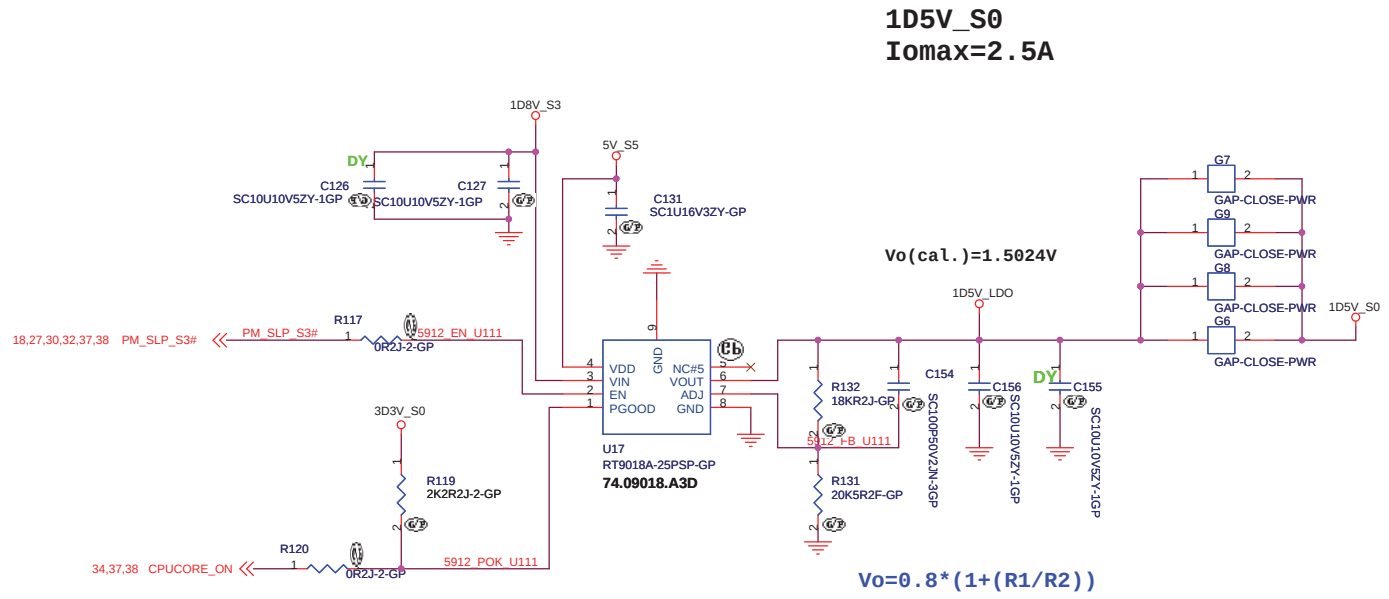


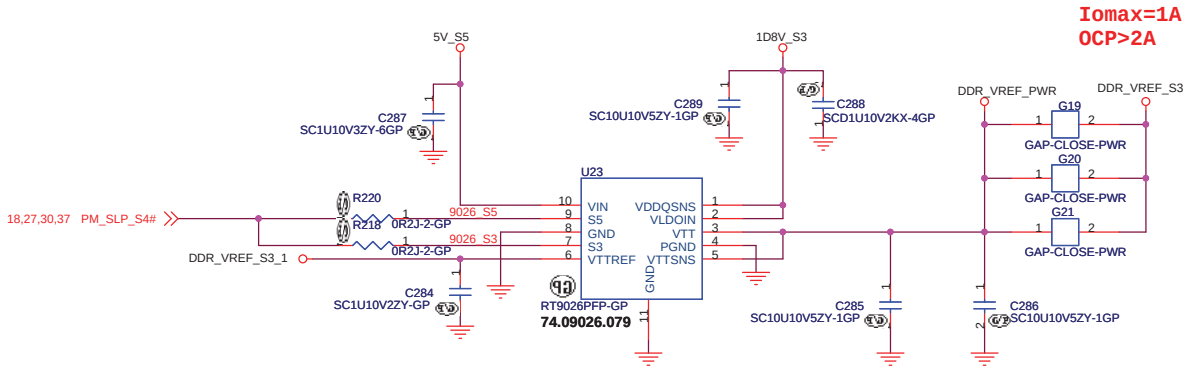
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**RUN POWER and 3D3V_AUX_S5**	
Size	Document Number **Cathedral Peak**	Rev SA
Date: Monday, January 14, 2008	Sheet 32 of 41	


CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
TPS51125
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
DCBATOUT_51125
PM_SLP_S4#
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (6A)
RT9018A
1D5V_S0
VIN
EN
1D5V(O)
PGOOD
1D8V_S3
PM_SLP_S3#
1D5V_S0 (2.5A)
CPUCORE_ON
RT9026
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S4#
0D9V_S3 (1A)
0D9V_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(5.5A)
G9131
2D5V_S0
INPUT
OUT
3D3V_S0
2D5V_S0(0.3A)
Charger BQ24750
Input Signal
CHGEN#
CELLS
Output Signal
ACGOOD#
SRSET
Input Power
ACN
Output Power
VOUT (O)
VOUT (O)
CHG_ON#
24750_CELLS
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D8V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D8V_S3 (10A)
1D05V_S0 (15A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
Cathedral Peak
Rev
SA
Date: Wednesday, November 14, 2007
Sheet 33 of 41

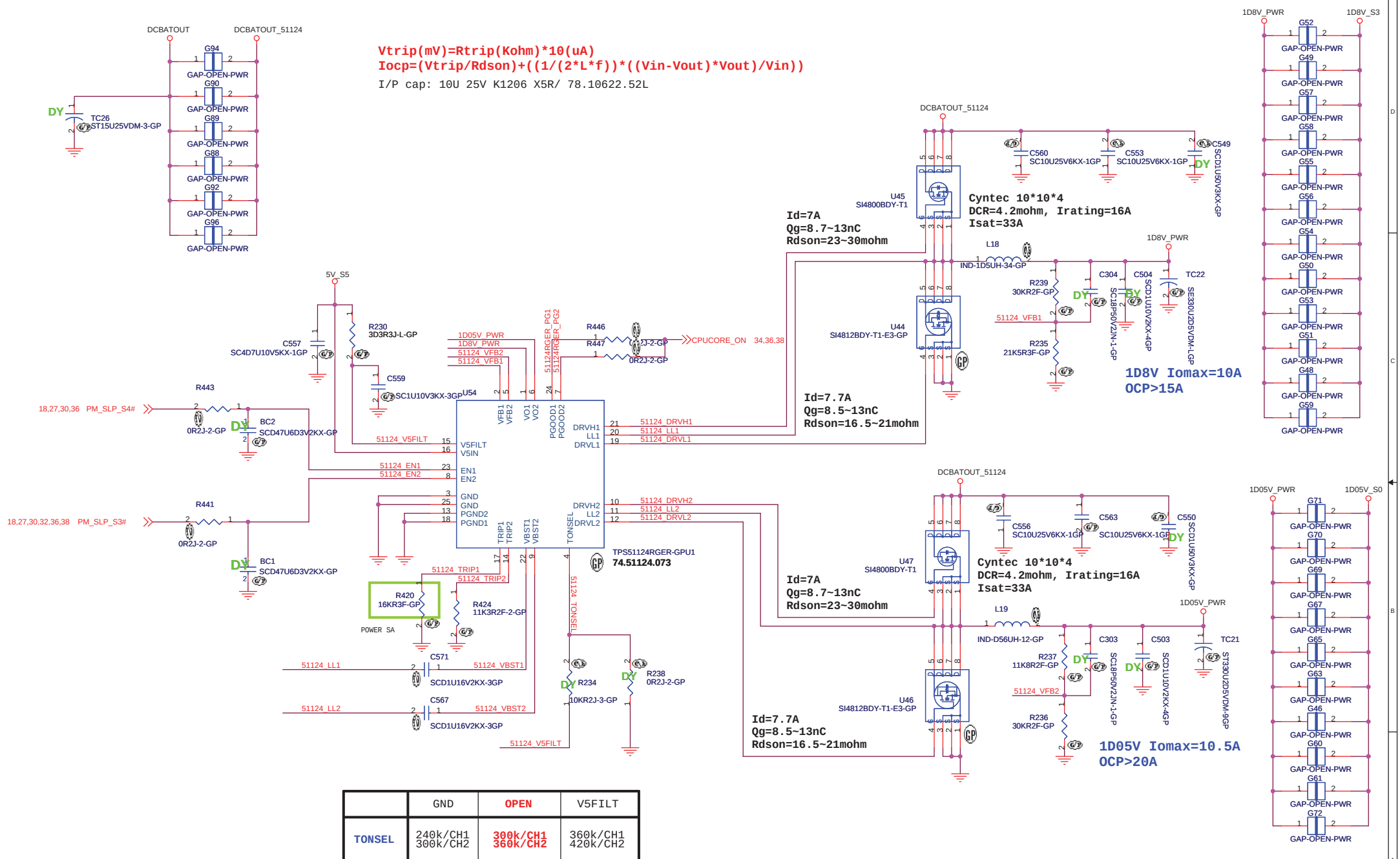

ISL6266AHRZ-GP
74.06266.073
U5
Vcc_core
Iomax=38A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
POWER SA
VCC_CORE
DCBATOUT_6266A
3D3V_S0
1D05V_S0
5V_S0
DCBATOUT
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC#25
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND
VDD
ISEN2
ISEN1
6266A_UGATE1
6266A_PHASE1
6266A_LGATE1
6266A_UGATE2
6266A_PHASE2
6266A_LGATE2
6266A_VSUM
6266A_ISEN1
6266A_VO
6266A_ISEN2
6266A_ISEN1_P1_VCORE
6266A_ISEN2_P1_VCORE
6266A_ISEN2_P2_VCORE
6266A_ISEN1_P2_VCORE
6266A_VSUM_R_VO
VCC_SENSE
VSS_SENSE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A CPU CORE
Size A3
Document Number
Cathedral Peak
Rev SA
Date: Friday, January 11, 2008
Sheet 34 of 41


DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
POWER SA
5V_PWR
5V_S5
5V_AUX_S5
51125_ENTIP2
51125_ENTIP1
S5_ENABLE
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=5A
U37
TPS51125RGER-GP
74.51125.073
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VREG3
VREG5
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
51125_VREF
TPAD28
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size A3
Document Number
Cathedral Peak
Rev SA
Date: Monday, January 14, 2008
Sheet 35 of 41





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**1D5V & 0D9V**	
Size A3	Document Number **Cathedral Peak**	Rev SA
Date: Friday, January 11, 2008	Sheet 36 of 41	



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D05V

Size: A3 | Document Number: Cathedral Peak | Rev: SA

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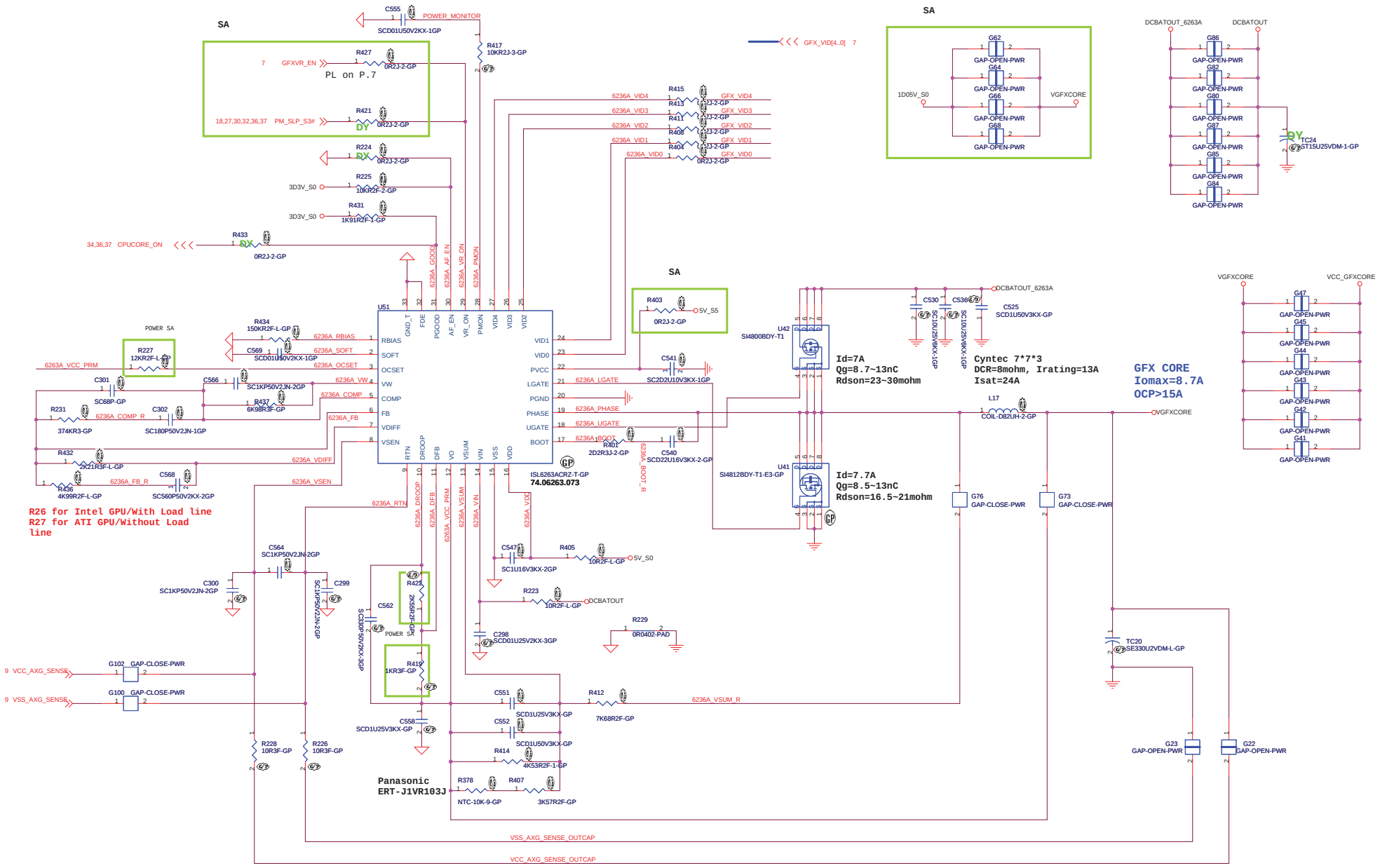

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Title: ISL6263A_GFX CORE

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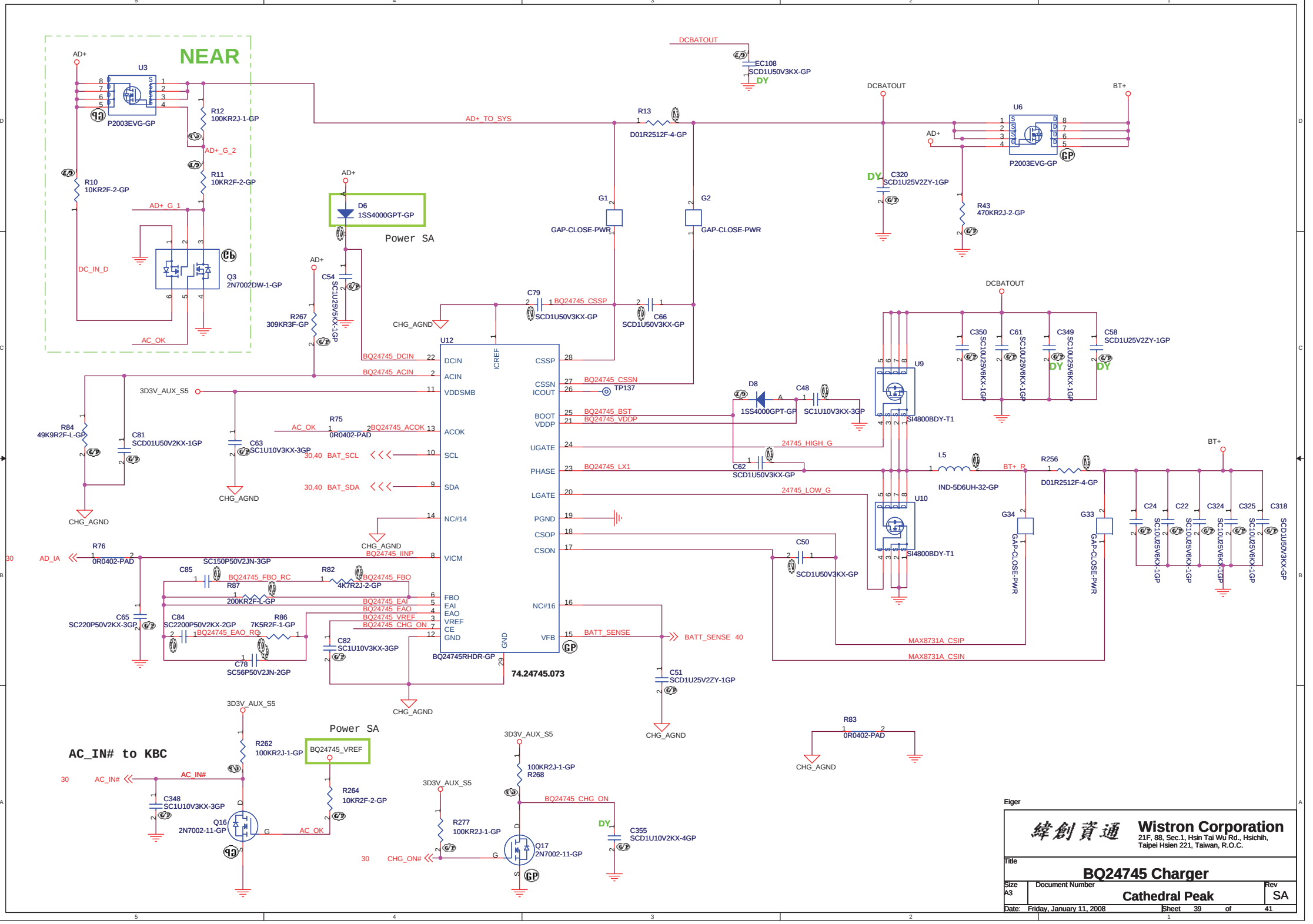
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R12
100KR2J-1-GP
AD+_G_2
R11
10KR2F-2-GP
R10
10KR2F-2-GP
AD+_G_1
DC_IN_D
Q3
2N7002DW-1-GP
AC_OK
D6
1SS4000GPT-GP
Power SA
C54
SC1U25V5KX-1GP
R267
309KR3F-GP
CHG_AGND
AD+_TO_SYS
R13
D01R2512F-4-GP
DCBATOUT
EC108
SCD1U50V3KX-GP
DY
G1
GAP-CLOSE-PWR
G2
GAP-CLOSE-PWR
C79
SCD1U50V3KX-GP
BQ24745_CSSP
C66
SCD1U50V3KX-GP
U6
P2003EVG-GP
BT+
C320
SCD1U25V2ZY-1GP
R43
470KR2J-2-GP
U12
BQ24745RHDR-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSN
TP137
BQ24745_BST
BQ24745_VDDP
BQ24745_ACOK
BQ24745_LX1
24745_HIGH_G
24745_LOW_G
BQ24745_IINP
BQ24745_FBO_RC
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BQ24745_EAO_RC
BATT_SENSE
BATT_SENSE_40
MAX8731A_CSIP
MAX8731A_CSIN
74.24745.073
3D3V_AUX_S5
R84
49K9R2F-L-GP
C81
SCD01U50V2KX-1GP
C63
SC1U10V3KX-3GP
R75
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30,40 BAT_SDA
R76
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AD_IA
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R87
200KR2F-1-GP
R82
4K7R2J-2-GP
C65
SC220P50V2KX-3GP
C84
SC2200P50V2KX-2GP
R86
7K5R2F-1-GP
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SC1U10V3KX-3GP
C62
SCD1U50V3KX-GP
C50
SCD1U50V3KX-GP
U9
SI4800BDY-T1
U10
SI4800BDY-T1
L5
IND-5D6UH-32-GP
BT+_R
R256
D01R2512F-4-GP
G34
GAP-CLOSE-PWR
G33
GAP-CLOSE-PWR
C350
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C24
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C324
C325
C318
SCD1U50V3KX-GP
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30
AC_IN#
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C348
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CHG_ON#
R268
100KR2J-1-GP
BQ24745_CHG_ON
C355
SCD1U10V2KX-4GP
Q17
2N7002-11-GP
Elger
緯創資通
Wistron Corporation
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Title
BQ24745 Charger
Size
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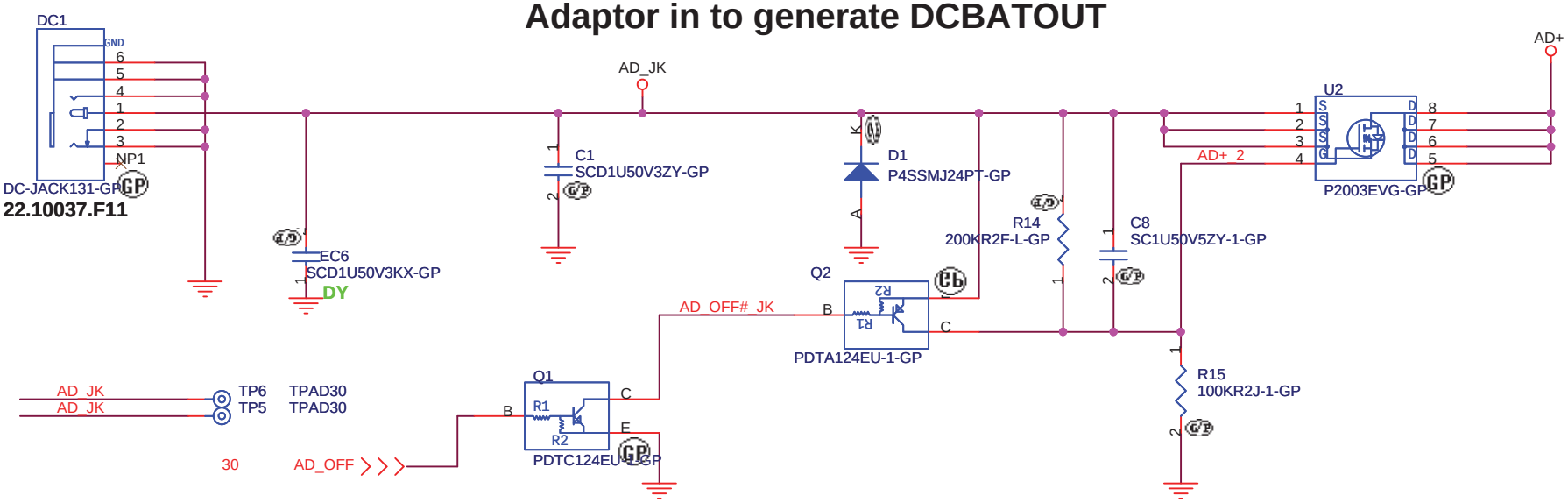
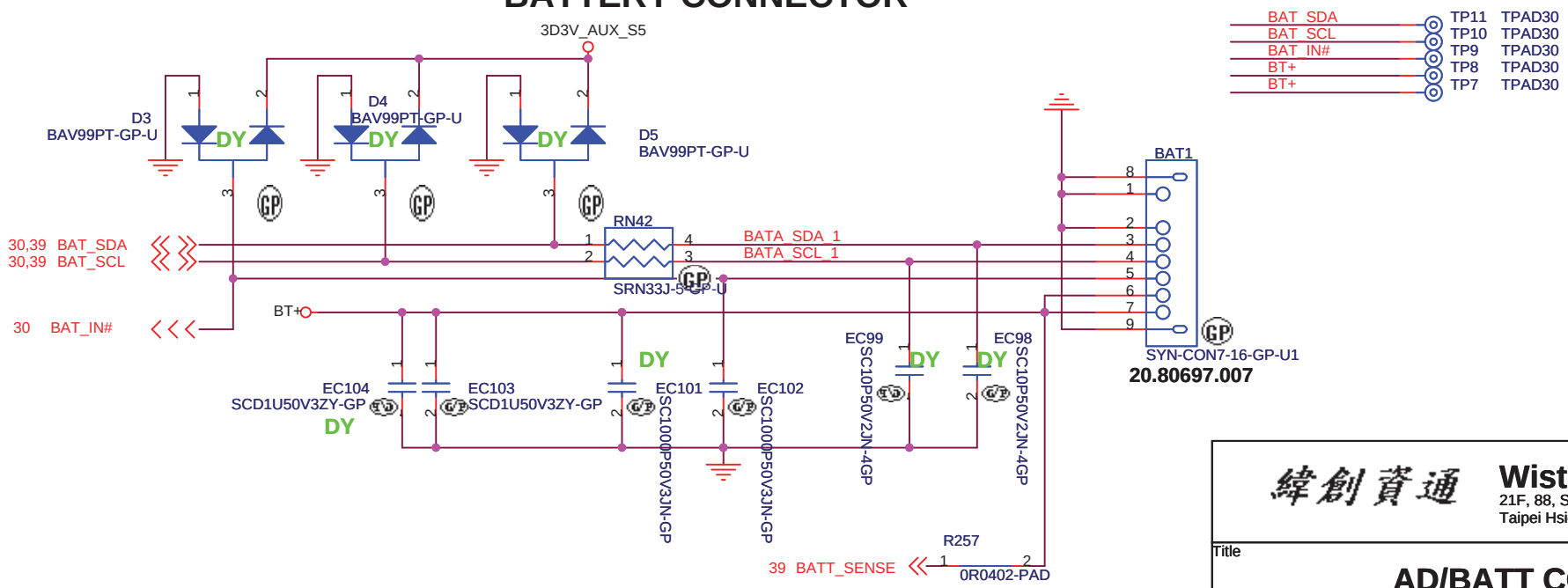
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title		
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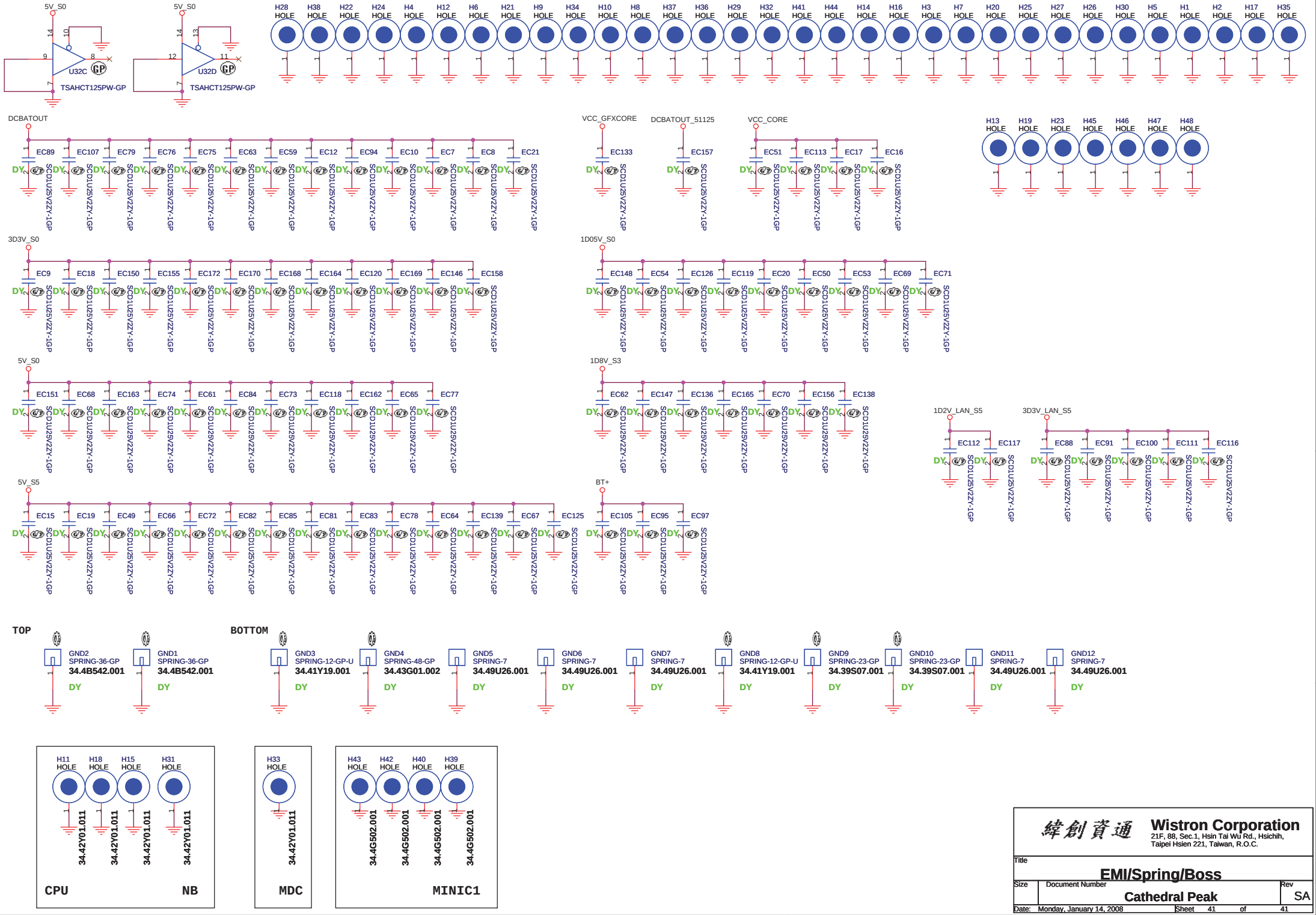

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